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Work Function Modulation Using Thin Interdiffused Metal Layers for Dual Metal-Gate Technology

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1. Introduction

Metal gates are required to boost transistor performance for the 32 nm complementary metal-oxide-semiconductor (CMOS) technology node and beyond. Interdiffusion of metal layers is one of the approaches explored for the realization of dual work function metal gate technology. Interdiffusion of Ni-Ti [1], Ni-Al [2], Ti-Pt, and Ti-W [3] has been reported. Recently, work function Φ_m tunability was achieved by inserting thin metal layers at the metal gate/dielectric interface [3]-[4]. Therefore, to achieve a well-controlled gate Φ_m with minimum spatial non-uniformity, thin metal layers with accurate thicknesses should be used for metal interdiffusion. In this work, we investigate the interdiffusion of thin metallic layers (≤10 nm) for work function modulation, employing elemental metal (Ni, Pt and Hf) and metal alloys (Ni-Hf and Pt-Hf). The dependences of Φ_m on metal thickness ratios and anneal temperatures were also investigated.

2. Experiment

The integration scheme for realizing dual gate work function using metal interdiffusion is shown in Fig. 1. The fabricated MOS capacitors employed either a SiO_2 gate dielectric (4 – 8 nm) or a HfO_2 (2 nm)/SiO_2 (4 – 8 nm) dielectric stack. The gate electrode comprises a bottom-most metal 1 layer on which a metal 2 layer is deposited. Table I shows the various combinations of the metallic materials investigated. In one set (shaded), metal 1 is a higher Φ_m metal, while metal 2 is a lower Φ_m metal. In another set (unshaded), metal 1 is a lower Φ_m metal alloy, while metal 2 is a higher Φ_m metal. Different metal 2/metal 1 thickness ratios (T_{Metal2}/T_{Metal1}) were used. All metals and metal alloys were deposited by sputtering and co-sputtering, respectively. Reactive-sputtered TaN (~100 nm) was used as the capping layer. After gate patterning, forming gas anneal (FGA) at 420 °C for 30 min or rapid thermal annealing (RTA) at 500 – 700 °C for 30 s in N_2 ambient was performed for metal interdiffusion. The atomic concentrations of $Ni_{0.66}Hf_{0.34}$ and $Pt_{0.71}Hf_{0.29}$ alloys (used for metal 1) were obtained by X-ray photoelectron spectroscopy (XPS). For example, the XPS spectra of Ni 2*p* and Hf 4*f* peak from $Ni_{0.66}Hf_{0.34}$ alloy is shown in Fig. 2.

3. Results and Discussions

Interdiffusion of Hf/Ni and Ni/Ni-Hf Stacks

Fig. 3 (a) shows the *C-V* curves of Hf/Ni interdiffused stacks after FGA. Fig. 4 (a) and (b) shows the secondary ion mass spectroscopy (SIMS) depth profile of a Hf/Ni stack before and after FGA. By increasing the Hf/Ni thickness ratio (T_{Hf}/T_{Ni}), the flatband voltage V_{FB} decreases with respect to that of the Ni stack. We found that the interdiffused layer has a higher Hf content when the T_{Hf}/T_{Ni} ratio is larger. In the case of the Ni/Ni-Hf stacks, however, varying of the T_{Ni}/T_{NiHf} ratio did not result in a significant V_{FB} shift as compared to that of the Ni/Hf stack [Fig. 3 (b)]. The SIMS profile of Ni/Ni-Hf stack (not shown) indicated minimal Ni diffusion after FGA. Hf/Ni and Ni/Ni-Hf stacks exhibited similar V_{FB} shifts after 500 °C RTA.

Interdiffusion of Hf/Pt and Pt/Pt-Hf Stacks

Hf/Pt and Pt/Pt-Hf stacks were investigated and their *C-V* curves after FGA are shown in Fig. 5. V_{FB} shifts for both stacks (compared with Pt or Pt-Hf gates) indicated that interdiffusion had taken place. Hf/Pt and Pt/Pt-Hf stacks were also subjected to higher RTA conditions due to their better thermal stability. Fig. 6 generally shows that larger V_{FB} shifts are observed at higher anneal temperatures. This is attributed to more interdiffusion occurring between the metal layers.

Summary of Extracted Φ_m

V_{FB} and equivalent oxide thickness T_{ox} obtained from the *C-V* curves were plotted to extract the metal gate Φ_m (Fig. 7). Φ_m variation for Hf/Pt and Pt/Pt-Hf stacks subjected to different anneal conditions, was also observed from the V_{FB} vs T_{ox} plots (Fig. 8). Fig. 9 shows the Φ_m tunability of the metal stacks. After FGA, the Φ_m of Hf/Ni interdiffused stack was tuned down from 4.74 eV (Ni stack) to 4.20 eV by varying the T_{Hf}/T_{Ni} ratio. After 700 °C RTA, Hf/Pt (Φ_m = 4.55 eV) and Pt/Pt-Hf (Φ_m = 4.90 eV) interdiffused stack gave the largest Φ_m shift (~0.5 eV) from their respective single layer gate stack. Finally, Fig. 10 shows the Φ_m of Ni, Pt, Ni-Hf and Pt-Hf gate stacks on both SiO_2 and HfO_2 gate dielectrics. This indicated that work function modulation of interdiffused metal layers can also be achieved on HfO_2 dielectric.

4. Conclusions

Thin interdiffused metal layers (≤10 nm) were implemented for Φ_m modulation. After FGA, Φ_m ranging between 4.20 – 4.74 eV was obtained for a Hf/Ni stack by varying the T_{Hf}/T_{Ni} ratio. Hf/Pt and Pt/Pt-Hf stacks showed better thermal stability and gave a Φ_m difference of ~0.5 eV from their single layer stack, after 700 °C RTA. With further process optimization, precise metal gate Φ_m control for advanced transistor structures can be achieved using this dual gate integration technique.

Acknowledgements

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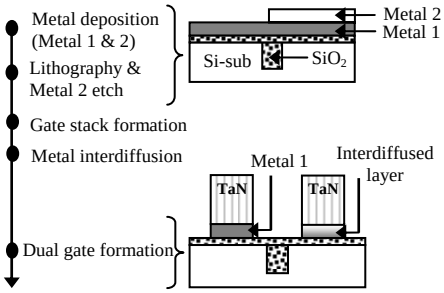

Fig. 1: Dual gate work function integration scheme making use of metal interdiffusion.

Table I: Experimental splits for MOS capacitors with interdiffused metal gates. Metal 1 was either a higher Φ_m metal (shaded) or a lower Φ_m metal alloy (unshaded).

Metal 2 (T_{Metal2})	Metal 1 (T_{Metal1})	T_{Metal2}/T_{Metal1}
Hf (7.0 nm)	Ni (5.0 nm)	1.40
Hf (7.0 nm)	Ni (10.0 nm)	0.70
Hf (3.5 nm)	Ni (10.0 nm)	0.35
Hf (7.0 nm)	Pt (10.0 nm)	1.40
Ni (10.0 nm)	Ni-Hf (5.0 nm)	2.00
Ni (5.0 nm)	Ni-Hf (5.0 nm)	1.00
Pt (10.0 nm)	Pt-Hf (5.0 nm)	2.00

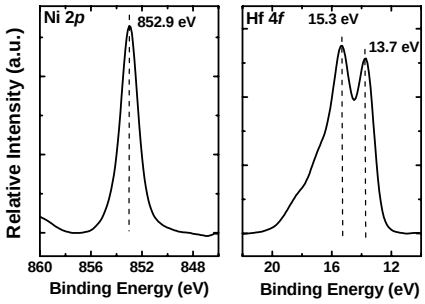

Fig. 2: XPS spectra of Ni 2*p* and Hf 4*f* from co-sputtered $Ni_{0.66}Hf_{0.34}$ alloy film.

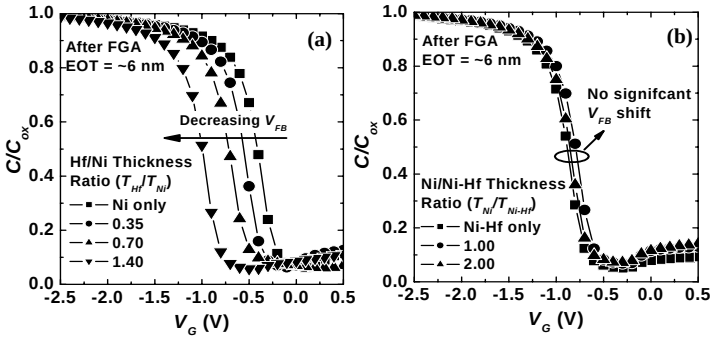

Fig. 3: *C-V* curves of (a) Hf/Ni and (b) Ni/Ni-Hf stacks after FGA. TaN-capped Ni (10 nm) and Ni-Hf (5 nm) stacks were used as reference.

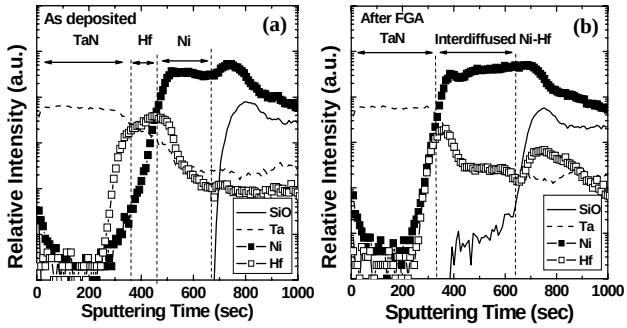

Fig. 4: SIMS depth profile of TaN (15 nm)/Hf (7 nm)/Ni (10 nm)/SiO_2 gate stack (a) before and (b) after FGA. A thinner TaN capping layer was used for ease of depth profiling.

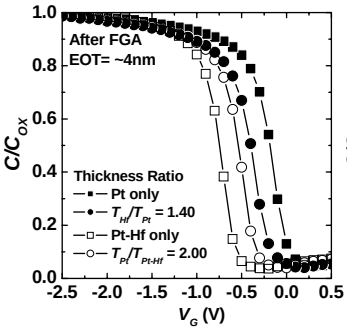

Fig. 5: *C-V* curves of Hf/Pt and Pt/Pt-Hf stacks after FGA. TaN-capped Pt (10 nm) and Pt-Hf (5 nm) stacks were used as reference.

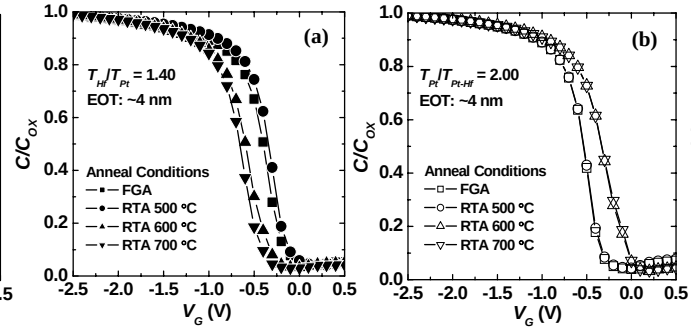

Fig. 6: *C-V* curves of (a) Hf/Pt and (b) Pt/Pt-Hf stacks after different anneal conditions. Larger V_{FB} shifts were observed at higher anneal conditions due to more interdiffusion of Hf and Pt, for Hf/Pt and Pt/Pt-Hf stacks, respectively.

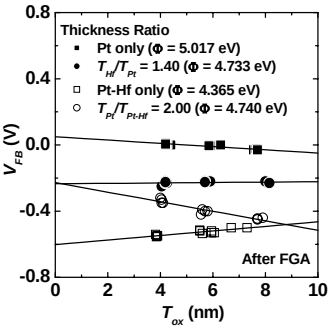

Fig. 7: V_{FB} vs T_{ox} plot used to extract the metal gate Φ_m.

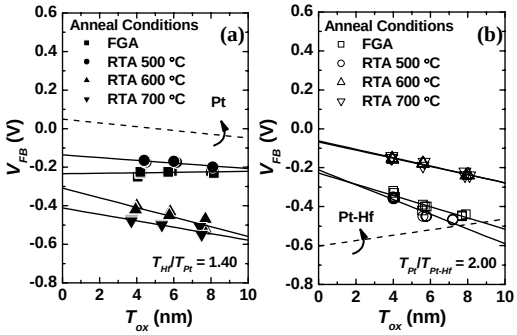

Fig. 8: V_{FB} vs T_{ox} plots of (a) Hf/Pt and (b) Pt/Pt-Hf stacks after different anneal conditions. TaN-capped Pt and Pt-Hf stacks after FGA are plotted as reference.

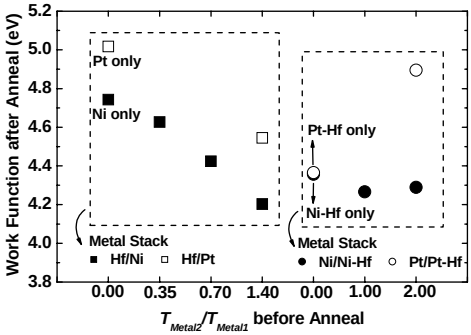

Fig. 9: Summary of Φ_m for all metal stacks. Hf/Pt and Pt/Pt-Hf stacks underwent 700 °C RTA while rest of the metal stacks underwent FGA.

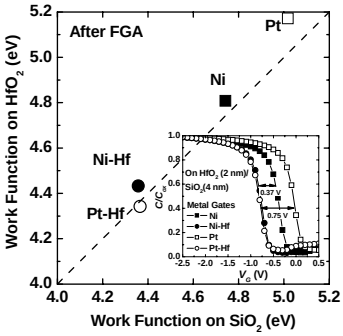

Fig. 10: Comparison of Φ_m on SiO_2 and HfO_2. Inset shows the *C-V* curves employing HfO_2 (2 nm)/SiO_2 (4 nm) dielectric.