Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 436-437

P-1-18

Ta/Mo Stack Dual Metal Gate Technology Applicable to Gate-First Processes

T. Matsukawa, Y.X. Liu, K. Endo, M. Masahara, K. Ishii, H. Yamauchi, J. Tsukada, and E. Suzuki
Nanoelectronics Research Institute, AIST, 1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan
Phone: +81-29-861-5358, Fax: +81-29-861-5170, E-mail: t-matsu@aist.go.jp

1. Introduction

Metal gate technology is essential to overcome gate depletion and boron penetration problems of poly-silicon gates. Though dual work functions (WFs) appropriate for both n- and p-MOSFETs in CMOS devices is necessary, process integration of the dual metal gates is a challenging issue. A fully silicided (FUSI) gate with dopant segregation is a candidate for the dual metal gate process [1]. However, this technology still suffers from the Fermi level pinning on high-k dielectrics due to Si contained in the silicide gate [2].

It was previously reported that interdiffusion of different metals stacked can provide different WFs for n- and p-MOSFETs without an etch-off process of an unnecessary metal from either n- or p-MOS region [3,4]. However, thermal robustness of the metals reported so far is not sufficient for a usable gate first process. In this paper, we select Mo and Ta with high (4.95 eV) and low (4.25 eV) WFs [5] for the interdiffusion dual-metal gate process. Ta and Mo are possible to pattern with a reactive ion etching (RIE) and are expected to have high thermal stability. We experimentally demonstrate the WF controllability of the Mo and Ta/Mo stack dual metal gates and confirm the sufficient thermal stability for the gate first processes.

2. Sample preparation

MOS capacitors with a single Mo layer and a Ta-on-Mo stack were fabricated though the processes shown in Fig.1. Deposition of the Mo layer on the SiO_2 gate dielectrics was carried out by e-beam evaporation or sputtering for comparison. For the case of the Ta/Mo stack, Ta (46 nm) was deposited by e-beam evaporation after the deposition of Mo (10 nm). After the gate patterning by RIE using SF_6 plasma, interdiffusion annealing (IDA) was carried out in vacuum to enhance the Ta diffusion into the Mo layer, followed by forming gas (3% H_2) annealing (FGA) at 450^{o}C for 30 min.

3. Results and Discussion

The cross-section of the Ta/Mo stack [Fig.2(a)] shows that the Ta and Mo layers were deposited homogeneously. The profiles of Mo and Ta across the Ta/Mo stack were explored by an EDX analysis and compared for different anneal conditions as shown in Figs. 2(b)-(d). After the FGA at 450^{o}C for 30 min., the diffusion of Ta into the Mo layer is recognized [Fig.2(c)] in comparison with the as-deposited sample [Fig.2(b)]. The additional IDA at 800^{o}C enhances the Ta diffusion [Fig.2(d)].

The C-V curves of the Mo and Ta/Mo gate samples prepared by e-beam evaporation of Mo are compared in Fig.3. The IDA was carried out at 700^{o}C for 1h. It is shown in Fig.3 that the different flat band voltage (Vfb) is obtained for the Mo and Ta/Mo gates, and the difference (ΔVfb) amounts to 0.43 V. However, the maximum capacitance at the accumulation shows the difference between the Ta and Ta/Mo gates, which means the capacitance equivalent thickness difference (ΔCET) of 0.74 nm. The Mo and Ta/Mo gate samples prepared by sputtering Mo (Fig.4) show the ΔVfb of 0.39 V. The maximum capacitance of both the samples is almost the same and the ΔCET of 0.13 nm is negligibly small.

The effective work functions (EWFs) of the Mo and Ta/Mo gates were estimated from the Vfb-CET plot as shown in Fig.5. The EWF change as a function of the IDA temperature is shown in Fig.6. For both the Mo gated capacitors by e-beam evaporation and sputtering, the EWF decreases remarkably with the IDA at 800^{o}C. Thus, the optimum IDA temperature is 700^{o}C or less. In this condition, the EWF difference between the Mo and Ta/Mo capacitors is 0.47 eV for the e-beam evaporated Mo sample and is 0.31 eV for the sputtered Mo one.

The thermal stability of the Mo and Ta/Mo gates was evaluated in terms of the CET change during the IDA at 600~900^{o}C. The CET values for the capacitors with the 5nm-thick thermal oxide are shown in Fig.7. The CET of the Mo gates increases with increasing IDA temperature, while that of the Ta/Mo gates decreases. It is noteworthy that the CET change is less significant for the sputtered Mo sample than that for the e-beam evaporated Mo sample. In the IDA range of 600~700^{o}C, the CET difference between the Mo and Ta/Mo gated capacitors prepared by the Mo sputtering is negligible. It is concluded that the sputtered Mo gated capacitors have the higher thermal stability.

The robustness against the thermal budget necessary for the gate-first process was examined. As a sufficient thermal budget for the source/drain activation [6], the rapid thermal annealing (RTA) at 850^{o}C for 20 sec. was carried out after the IDA at 600^{o}C for 1h for the samples prepared by the Mo sputtering. As shown in Fig.8, the sufficient amount of ΔVfb (0.39 V) remains after the RTA, and the CET difference between the Mo and Ta/Mo gated samples keeps a insignificant level (0.4 nm). Thus, we conclude that the Mo and Ta/Mo gates are promising as the dual metal gates and are applicable to the gate-first CMOS processes.

4. Conclusions

We have studied Mo and Ta/Mo gates as candidates of the dual work function metal gates. In the Ta/Mo stack gate, Ta diffusion into the Mo layer gives lower work function than the Mo single layer gate. Actually, the annealing at 600~700^{o}C gives the sufficient WF difference (0.31~0.47 eV) between the Mo and Ta/Mo gates. The thermal robustness of the Mo and Ta/Mo gates prepared by Mo sputtering is superior than that by e-beam evaporation of Mo, and the robustness against RTA at 850^{o}C for 20 sec. is also confirmed. Thus, the combination of the Mo and Ta/Mo gates is one of the candidates for the dual work function metal gates acceptable to the gate-first CMOS processes.

References

[1] J.Kedzierski *et al*., *IEDM Tech. Dig*., (2003) 315.
[2] T.Nabatame *et al*., *IEDM Tech. Dig.*, (2004) 83.
[3] I.Polishchuk *et al*., *IEEE Electron Dev. Lett.*, 22 (2001) 444.

[4] T.Matsukawa *et al*., *Appl. Phys. Lett.*, 86 (2005) 094104.
[5] H.Michaelson, *J. Appl. Phys.*, 48 (1977) 4729.
[6] R.Lindsay *et al*., *Extended Abstract of IWJT*, (2004) 70.

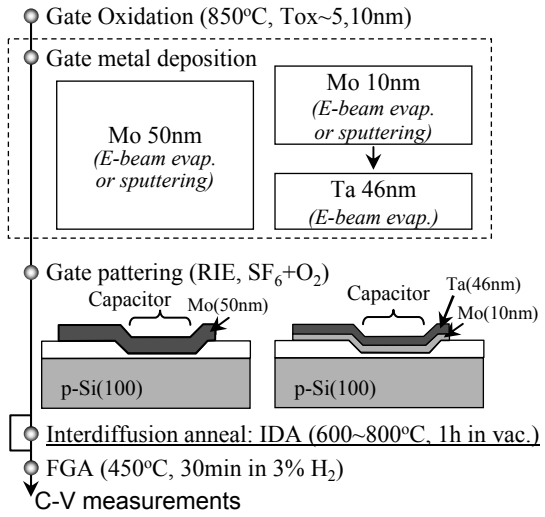

Fig.1 Process flow for the Mo and Ta/Mo MOS capacitors.

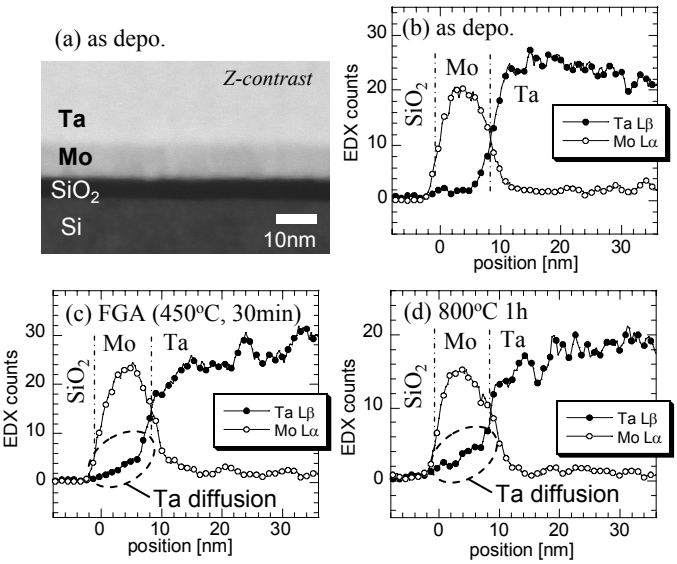

Fig.2 Ta diffusion into the Mo layer analyzed by STEM and EDX. (a) cross sectional view of the Ta/Mo stack MOS capacitor before IDA. Distribution of Ta and Mo for the samples: (b) as deposited, (c) after PMA at 450°C, and (d) after IDA at 800°C.

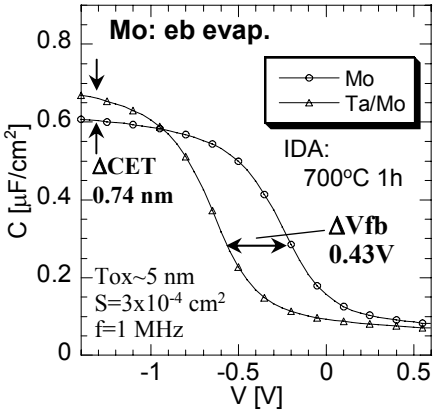

Fig.3 C-V curves of Mo and Ta/Mo gates with IDA (700°C, 1h). Mo layers were deposited by e-beam evaporation.

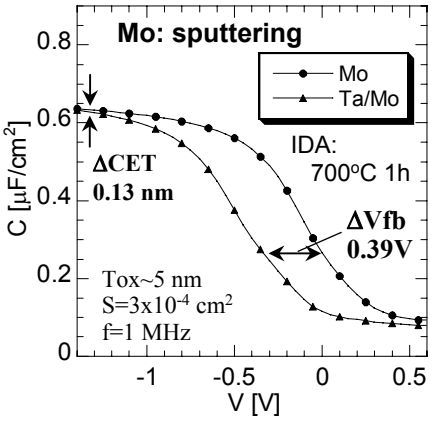

Fig.4 C-V curves of Mo and Ta/Mo gates with IDA (700°C, 1h). Mo layers were deposited by sputtering.

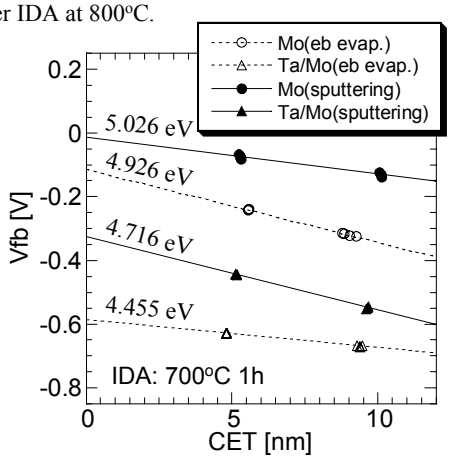

Fig.5 Vfb-CET plot for work function estimation. Different work functions for Mo and Ta/Mo gates were obtained.

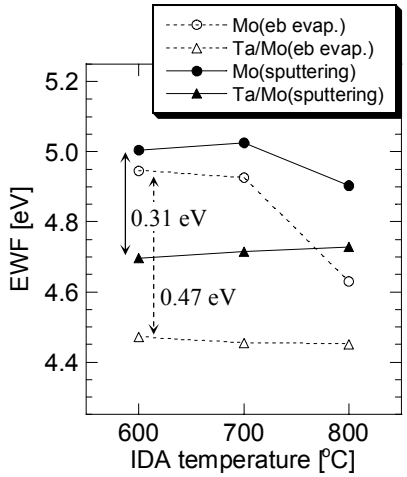

Fig.6 Influence of IDA temperature on EWFs of Mo and Ta/Mo MOS capacitors.

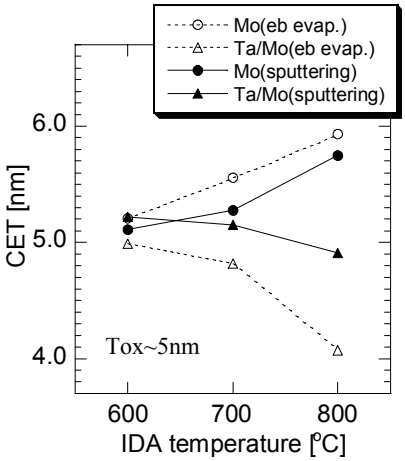

Fig.7 Influence of IDA temperature on CET of Mo and Ta/Mo MOS capacitors made on 5nm-thick thermal oxide.

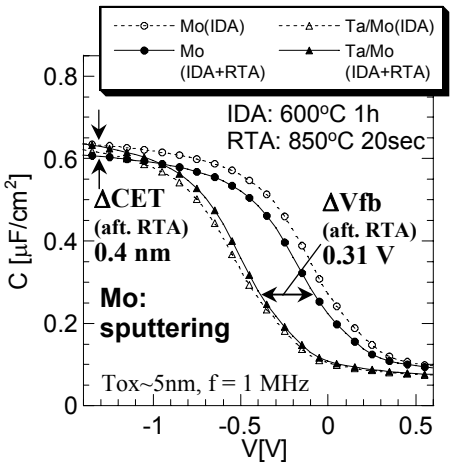

Fig.8 Influence of RTA (850°C 20 sec) on C-V curves of Mo and Ta/Mo MOS capacitors with sputtered Mo. ΔVfb of 0.31 V and ΔCET of 0.4 nm were ensured even after RTA.