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Physical and Electrical Characteristics of HfN Metal Gate Electrode Synthesized by Post-Rapid Thermal Annealing-assisted MOCVD

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1. Introduction

Continued scaling down of CMOS devices makes high-κ dielectric and metal electrode necessary to replace traditional SiO_2 dielectric and polysilicon gate electrode. Hafnium nitride (HfN) is one of the most promising candidates to replace polysilicon as a metal gate electrode because of its superior properties [1,2].

We have already reported that $HfN_{1.39}$ film with low levels of C (<0.1 at.%) and O (~2 at.%) impurities can be synthesized by MOCVD using $Hf[N(C_2H_5)_2]_4$ (TDEAHf) precursor and NH_3 gas, but the as-deposited films behave insulating characteristic due to the formation of N-rich Hf_3N_4 phase [3]. In this work, we develop a post-rapid thermal annealing (PRTA)-assisted MOCVD (PRTA-MOCVD) technique to synthesize pure HfN metal gate electrode. It is found that insulating $HfN_{1.39}$ films, formed by MOCVD, can be transformed into conductive HfN phase just by 1 min-PRTA process at about 1000 ^oC. The PRTA-MOCVD-HfN film has been evaluated as gate electrode applications. In addition, SiO_2 dielectric evolution after PRTA process, which results in the large reduction in EOT, has also been investigated.

2. Experimental

In this work, two sets of hafnium nitride samples are grown on SiO_2 (100 nm) for material characterization. One set is pure and insulating $HfN_{1.39}$ (200 nm) samples fabricated by MOCVD using TDEAHf precursor and NH_3 gas. The details of sample synthesis have been described in our previous report [3]. Another set is insulating $HfN_{1.44}$ (50-150 nm) reference samples prepared by DC sputtering. Because the study on hafnium nitride by CVD method is ongoing now, the well-know PVD synthesis (DC sputtering) is employed firstly to investigate the evolution of film structure and electrical property with post-rapid thermal annealing (PRTA). PRTA processes are carried out in a vacuum ambient with base-pressure below 10^{-5} Pa. The PRTA time is 1min, and PRTA temperature is arranged from 950 ^oC to 1100 ^oC.

Rutherford backscattering spectrometry (RBS) by an accelerator (NHV, AN-2500) with 2.0 MeV $^4He^{2+}$ particles are used to estimate the atomic composition. The sheet resistance of the films is measured using a four-point probe technique.

3. Results and discussion

According to the assessment in high pressure synthesis of Hf_3N_4 nitride [4], the phase boundary between metallic HfN and insulating Hf_3N_4 phases is accessed as a function of temperature and pressure, as shown in Fig. 1. Based on the stability viewpoint of Hf_3N_4 phase, PRTA process in vacuum ambient is carried out.

Firstly, PVD-$HfN_{1.44}$ samples are used to evaluate the possible phase transition and expected electrical property change. Figure 2 shows grazing-angle (1^o) incidence XRD patterns of the PVD-$HfN_{1.44}$ film after PRTA process at different process temperatures for 1 min. After the PRTA process, the peak shift from 33.1^o for the as-deposited film to 34.4^o for the PRTA films, and the newly emerging peaks at about 57.7^o and 68.9^o can be fully attributed to the formation of a new cubic NaCl-type HfN structure with a (111)-preferred orientation. To further prove this phase transition, electrical resistivity of the PVD-$HfN_{1.44}$ films subjected to PRTA is measured. The resistivity evolution of the films is shown in Fig. 3. After the PRTA process, film resistivity is dramatically decreased to the order of 10^3 μΩ-cm, implying the phase transition from insulating N-rich $HfN_{1.44}$ to conductive HfN. Composition identification is also carried out by RBS measurement. After 1000 ^oC PRTA process, the atomic ratio of N to Hf becomes 1.33, which is slightly lower than the original value of 1.44 for the as-deposited $HfN_{1.44}$ film. By means of thickness dependence evaluation of electrical resistance and resistivity for the samples subjected to PRTA as shown in Fig. 4, local layer phase-transformation is precluded, namely, the insulating $HfN_{1.44}$ film has been completely transformed into metallic HfN film. The excessive nitrogen may be most probably accommodated in the HfN crystal by occupying the intergranular and/or interstitial positions ways. So, it can be concluded that PRTA process is capable of synthesizing metallic HfN film. The mechanism of film synthesis is based on the thermodynamic equilibrium property of the Hf-N compounds.

Based on the above experimental conclusion, an identical PRTA process is performed on the CVD-$HfN_{1.39}$ films synthesized by MOCVD using TDEAHf precursor and NH_3 gas. PRTA can reduce the atomic ratio of N to Hf from 1.39 to 1.31. A series of similar results are obtained including structural and electrical analysis, indicating PRTA-MOCVD is an effective method to fabricate pure HfN metal gate electrode. This process is potentially compatible with the current CMOS device integration, because the highest temperatures used in device fabrication are for the activation of dopant atoms in the source and drain regions of the transistor. Typical activation thermal budgets include rapid thermal annealing at about 1000 ^oC for a few seconds to a minute. Activation of dopant atoms and metal HfN gate electrode transformation from N-rich CVD-$HfN_{1.39}$ counterpart are expected to be realized simultaneously.

In order to evaluate the electrical characteristic of the PRTA-MOCVD-$HfN_{1.31}$ film as metal gate electrode, MOS capacitors are produced using p-type Si (100) with different thickness of SiO_2 (~6.3, 8 and 9.5 nm). Table 1 summarizes the process flow of MOS capacitor structures with Ru/CVD-$HfN_{1.39}$ gate, which is subjected to 1000 ^oC PRTA. Figure 5 shows the high frequency C-V curves of the Ru/CVD-$HfN_{1.39}$ gated capacitors on SiO_2 after PRTA at 1000 ^oC for 1 min and FGA for 30 min sequentially. The inset shows the V_{fb} vs. EOT plot. Well behaved C-V curves indicate the good thermal stability and compatibility with pMOS devices for the PRTA-$HfN_{1.31}$ gate electrode even up to 1000 ^oC. This result is comparable with the amorphous metal-incorporated metal nitrides for nMOS devices application [5,6]. Compared with the 4.71 eV of effective work function for the PVD-HfN [7], the large effective work function for the PRTA-MOCVD-$HfN_{1.31}$ gate (near to 5.0 eV) can be attributed to the evolution of structural as well as chemical changes of the CVD-$HfN_{1.39}$ films during PRTA process. The preferred crystallization of the PRTA-MOCVD-$HfN_{1.31}$ and the grain boundary effect are believed to be responsible for the high work function. Densely packed crystallographic surfaces are expected to have high work function since these surfaces are relatively inert with fewer broken atomic bonds [8]; free electrons could be trapped in the grain boundaries and result in higher work function [9]. Figure 6 shows the leakage current properties of the PRTA-MOCVD-$HfN_{1.31}$ gated MOS capacitors. Low leakage currents indicate the good compatibility of PRTA process with MOS device integration. In addition, it must be noted that all the SiO_2 EOTs become smaller than those physical thickness after PRTA process, as shown in Fig. 7. This can be attributed to the formation of high-κ interlayer by consuming SiO_2 layer. If assuming the dielectric constant of the high-κ interlayer is 16, a series of simulated EOT plots can be obtained by assigning different interlayer thickness. Based on this consideration, the thickness of the high-κ interlayer is estimated to be about 3~4 nm. This result implies a potential possibility to further reduce the EOT, and even to 1 nm by employing PRTA process for the CVD- $HfN_{1.39}$ on SiO_2. Related work about it is ongoing now.

3. Conclusions

Physical and electrical characteristics of HfN metal gate electrode formed by PRTA process for the N-rich $HfN_{>1}$ films are studied. Phase transformation from insulating N-rich $HfN_{>1}$ into metallic HfN is confirmed at about 1000 ^oC. The PRTA-MOCVD-$HfN_{1.31}$ film shows effective work function of about 5.0eV, even after 1000 ^oC annealing. It also shows well behaved C-V and I-V characteristics, which suggest excellent compatibility with PMOS devices. In addition, SiO_2 EOT shrinkage due to the formation of high-κ interlayer also shows potential application prospect in CMOS device scaling.

References

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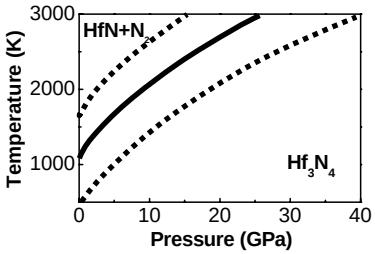

Fig. 1. Pressure-Temperature diagram of the chemical reaction $3Hf+0.5N_2 \rightarrow Hf_3N_4$. The solid curve corresponds to phase equilibrium ($\Delta G=0$); the dashed curves to $\Delta G=\pm 0.5$ (account for the uncertainties of calculation).[4)]

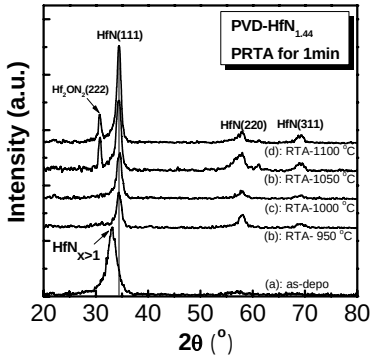

Fig. 2. XRD patterns of the PVD-$HfN_{1.44}$ films after PRTA process at 950°C, 1000°C, 1050°C and 1100°C for 1min, respectively. Grazing-angle incidence mode (1°) is used.

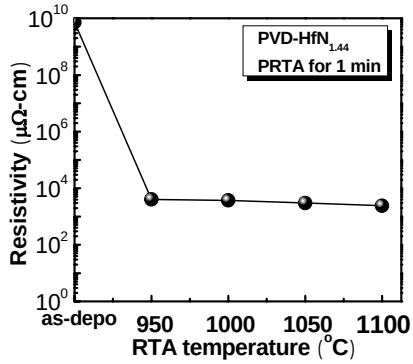

Fig. 3. Dependence of electrical resistivity on PRTA temperature for the PVD-$HfN_{1.44}$ films.

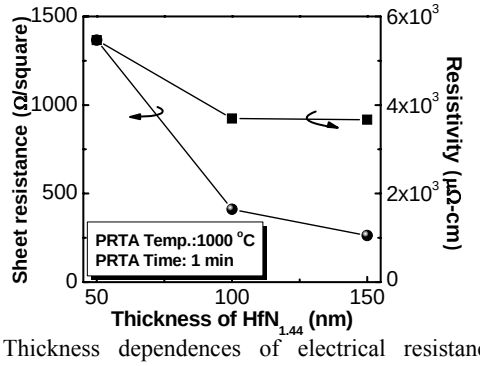

Fig. 4. Thickness dependences of electrical resistance and resistivity for the PVD-$HfN_{1.44}$ films after PRTA process at 1000 °C for 1 min. The film surface is oxidized slightly (about 10 nm).

Table 1. Process flow of PRTA-induced CVD-$HfN_{1.39}$ metal electrode gated MOS capacitor

SiO_2 dielectrics (6.3 nm-9.5nm)
Deposition of CVD-$HfN_{1.39}$ (200 nm)
Surface cleaning with buffered HF
Deposition of sputtering-Ru (70 nm)
PRTA process at 1000 °C for 1 min
Electrode patterning by dry etch
FGA process at 400 °C for 30 min
Evaluation of electrical properties

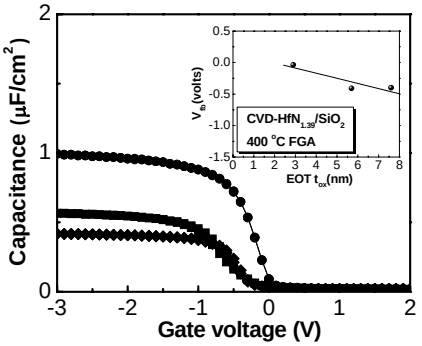

Fig. 5. High frequency C-V curves of the Ru/CVD-$HfN_{1.39}$ gated capacitors on SiO_2 with various thickness after PRTA at 1000 °C for 1 min and FGA at 400 °C for 30 min.

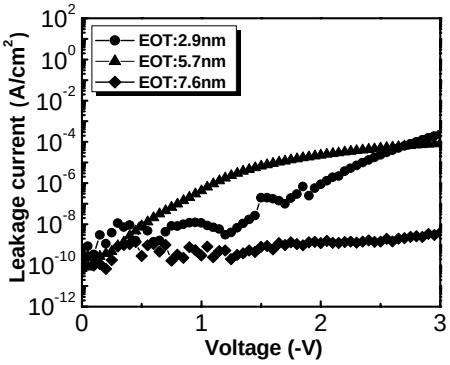

Fig. 6. Typical I-V curves of the Ru/CVD-$HfN_{1.39}$ gated capacitors on SiO_2 after PRTA and FGA processes.

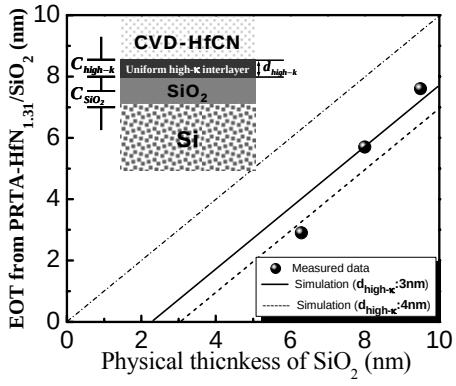

Fig. 7. EOT vs. SiO_2 film thickness plots for the PRTA-$HfN_{1.31}$ gated capacitors. Solid dots stand for the measured data; solid and dashed lines are from the simulation by assuming 16 of dielectric constant and different thickness for the high-κ interlayer. The inset shows the schematic diagram of high-κ interlayer hypothesis.