Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 454-455

P-1-27

Low Leakage Current and Low Resistivity p^+n Diodes on Si(110) Fabricated by Ga^+/B^+ Combination I/I and Low Temperature Annealing

Hiroshi Imai[1], Akinobu Teramoto[2], Shigetoshi Sugawa[1] and Tadahiro Ohmi[2]
[1]Graduate School of Engineering, Tohoku University, Sendai 980-8579, Japan
[2]New Industry Creation Hatchery Center, Tohoku University, Sendai 980-8579, Japan
Phone: +81-22-795-3977 Fax: +81-22-795-3986 e-mail: imai@fff.niche.tohoku.ac.jp

I. Introduction

For the improvement of current drivability of MOSFET, CMOS devices fabricated on Si(110) were reported in recent years [1,2]. And new materials such as high-κ gate dielectrics [3] and metal gate electrodes [4] are introduced to FEOL processes to overcome the scaling limit. In such cases, low temperature annealing process is necessary, especially low temperature source/drain activation annealing is required.

Solid Phase Epitaxial Regrowth (SPER) is well known way as low temperature source/drain activation technology [5]. However, it was reported in [6] that SPER on Si(110) is more difficult compared with Si(100). Fluorine knocked into amorphous layer formed by BF_2^+ ion implantation (I/I) prevents re-crystallization and activation of the implanted Boron on low temperature annealing [7]. In this paper, we studied other types of p^+ ion; Ga^+ I/I and Ga^+/B^+ combination I/I on Si(110) followed by low temperature annealing at 550°C.

II. Experimental conditions

Cz, n-type Si(110) with 8-12 [Ω-cm] and Cz, n-type Si(100) with 8-12 [Ω-cm] wafers are employed in the experiment.

To investigate the annealing behavior, Ga^+/B^+, Ga^+ and BF_2^+ ions were implanted on the bare *n*-Si(110) and *n*-Si(100) wafers followed by annealing at 450°C ~ 550°C. To measure electrical characteristics, 100um × 1000um rectangular p^+n junctions were fabricated by Ga^+/B^+ implantation followed by annealing at 550°C and fabricated by BF_2^+ implantation followed by 600°C annealing on Si(110) and Si(100), respectively. Each condition of the ion implantation is described in Table I.

Table I Conditions of p^+ ion implantation

Types of I/I	Times of I/I		
	1st.	2nd.	3rd.
Ga^+/B^+	Ga^+ 5 5×10^{13}	Ga^+ 43 2×10^{14}	B^+ 4 2×10^{15}
Ga^+	Ga^+ 10 1×10^{15}	Ga^+ 36 1×10^{15}	-
BF_2^+	BF_2^+ 25 2×10^{15}	-	Type of Ion Energy [keV] Dose [cm^{-2}]

III. Results and Discussions

Figure 1 shows the sheet resistance of Ga^+/B^+, Ga^+ and BF_2^+ implanted on Si(100) and (110) followed by annealing at 500°C and 550°C as a function of annealing time. Both Ga^+/B^+ implanted samples on Si(110) and (100) show saturation sheet resistance of below 200 [Ω/sq.] (164.7 [Ω/sq.] on Si(100), 198.7 [Ω/sq.] on Si(110)). The saturation resistance of the p^+ layer on Si(110) formed by Ga^+/B^+ with annealing at 550°C is lower than that of the p^+ layer formed by BF_2^+ implanted on Si(100). Fig. 2 shows the carrier concentration depth profiles of the Ga^+/B^+ implanted on Si(110) sample followed by annealing at 550°C and that of BF_2^+ implanted sample. The ^{11}B SIMS profile of the Ga^+/B^+ sample is also plotted. Surface carrier concentration of the Ga^+/B^+ implanted sample is higher than 2×10^{20} [cm^{-3}]. Figure 3 shows the average regrowth rate of the Ga^+/B^+ and BF_2^+ implanted amorphous layer as a function of annealing temperature. The result shows the SPER rates of Ga^+/B^+ implanted samples are higher than that of BF_2^+ implanted on Si(100) sample. Fig. 2 and Fig. 3 reveal that Ga^+/B^+ implantation without fluorine is very effective for low temperature annealing.

Figure 4 and 5 show the reverse and forward bias J-V characteristics of p^+n diodes fabricated by Ga^+/B^+ implantation on Si(110) followed by annealing at 550°C and formed by BF_2^+ implantation on Si(110) and Si(100) followed by annealing at 600°C, respectively. The reverse bias leakage current of the p^+n diode formed by Ga^+/B^+ implantation on Si(110) sample is less than 4.0×10^{-10} [A/cm^2] and the n-value shows ideal characteristic of diffusion current (n=1.00). The Arrhenius plots for the leakage current density measured at –1.00 [V] of the p^+n formed by Ga^+/B^+ implantation on Si(110) and Si(100) followed by annealing at 550°C and BF_2^+ implanted on Si(110) with 600°C annealing samples are shown in Fig. 6. The activation energy of Ga^+/B^+ implanted samples is 1.1 [eV] (= Si band-gap energy) until room temperature. It reveal that the defects in p^+n junction formed by Ga^+/B^+ implantation on Si(110) are annealed out well at 550°C. These show that the ideal p^+n junction can be realized by Ga^+/B^+ I/I followed by low temperature annealing at 550 °C. It is very useful for scaling down LSI devices.

IV. Conclusion

We have fabricated p^+n diode on Si(110) formed by Ga^+/B^+ combination ion implantation and low temperature annealing at 550°C. The surface carrier concentration of the formed p^+ layer exceeds 2.0×10^{20} [cm^{-3}], and which corresponds to below the resistivity of 7.0×10^{-3} [Ω-cm]. The reverse bias leakage current density of the p^+n diode is less than 4.0×10^{-10} [A/cm^2] at room temperature (298K). The forward bias current density of the p^+n diode shows ideal diffusion current density.

This paper gives the key technology of fabricating source/drain by low temperature annealing, especially on Si(110) surface. It is very effective for CMOS integration such as including high-κ gate dielectrics and metal gate electrodes in the devices.

References

[1]A. Teramoto, *et al., IEDM Tech. Dig.*, (2003) p. 801.
[2]B. Doris, *et al., VLSI symp. Tech. Dig.*, (2004) p. 86.
[3]E. Gusev, *et al., IEDM Tech. Dig.*, (2001) p. 451.
[4]J. K. Schaeffer, *et al., IEDM Tech. Dig.*, (2004) p. 287
[5]B. L. Crowder, *J. Electrochem. Soc.*, **118**, (1971) p. 943.
[6]L. Csepregi, *et al., J. Appl. Phys.* **48**, (1977) p. 4234
[7]A. Nakada, *et al., J. Appl. Phys.* **81**, (1997) p. 2560

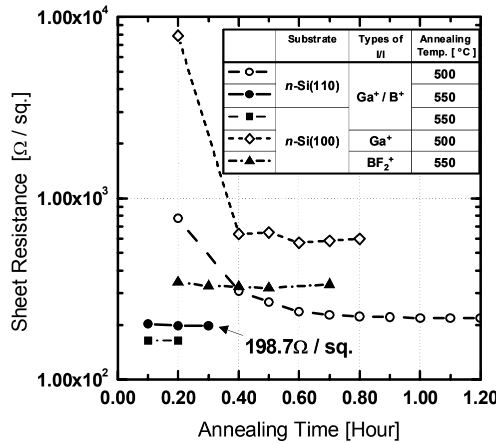

Fig. 1. Sheet resistance of Ga^+/B^+, Ga^+ and BF_2^+ implanted layers on *n*-Si(110) and *n*-Si(100) as a function of annealing time. Sheet resistnce obtained by the Ga^+/B^+ I/I on Si(110) and annealing at 550ºC is less than 200 [Ω/sq].

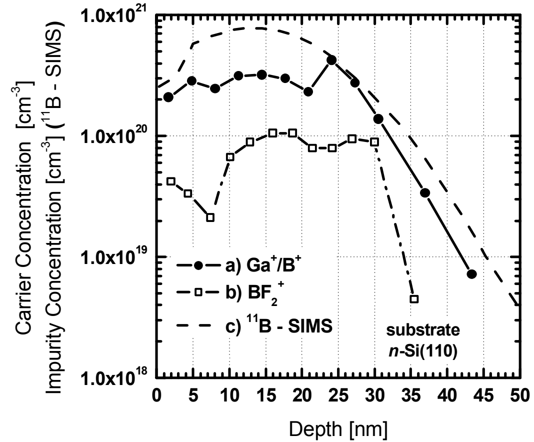

Fig. 2. Carrier concentration profiles of Ga^+/B^+ I/I (plot (a)), BF_2^+ Implanted (plot (b)) on *n*-Si(110) with annealing at 550°C, respectively. Plot (c) is a SIMS depth profile of ^{11}B on the same condition of the sample (a). The surface carrier concentration of the Ga^+/B^+ implanted sample is higher than 2.0×10^{20} [cm^{-3}].

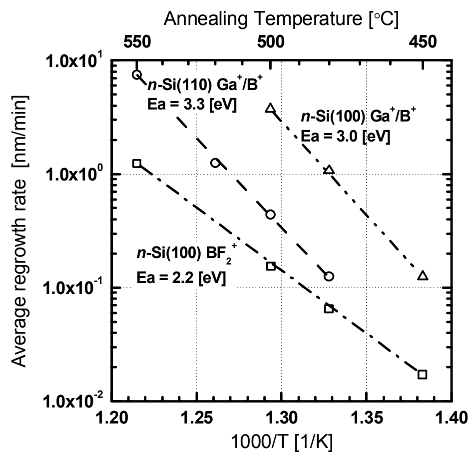

Fig. 3. Annealing temperature dependence of the average regrowth rate of the amorphous layer formed by Ga^+/B^+ implantation on *n*-Si(100), *n*-Si(110) and that of the BF_2^+ on *n*-Si(100) . The Average regrowth rate is defined as initial amorphized layer thickness / annealing time just after the saturation point of sheet resistance.

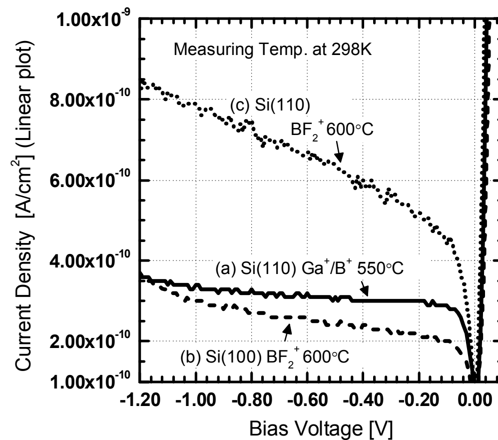

Fig. 4. J-V characteristics of the p⁺n diodes formed by Ga^+/B^+ I/I on Si(110) followed by annealing at 550°C, by BF_2^+ I/I on Si(110) with 600°C annealing and that of on Si(100), respectively. The reverse bias leakage current of the diode by Ga^+/B^+ I/I on Si(110) is reduced as low as that of 600°C annealing on Si(100) sample.

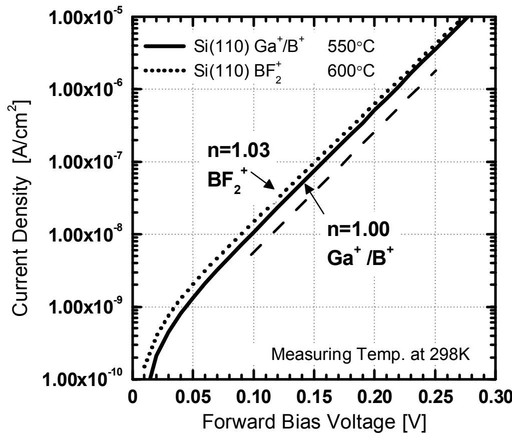

Fig. 5. Current - forward bias voltage characteristics of the p^+n diodes fabricated by the same conditions as (a) and (c) in Fig.4. The p^+n diode fabricated by Ga^+/B^+ implantation shows ideal n-value = 1.00 and it reveals that the defects in the diode are saficiently annealed out at 550°C.

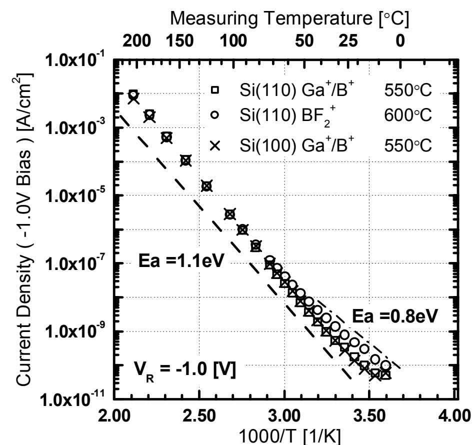

Fig. 6. Arrhenius plots for reverse-bias current density measured at -1.00 [V] of formed by Ga^+/B^+ implantation on Si(110) with 550°C annealing and that of on Si(100), by BF_2^+ implantation on Si(110) followed by annealing at 600°C, respectively. The junctions fabricated by Ga^+/B^+ I/I shows ideal activation energy even below 298[K].