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Epitaxial High-K Oxide Metal Gate MOSFETs: Damascene CMP Process Integration and Electrical Results

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1. Introduction

Ever increasing gate leakages through ultra-scaled SiO_2 gate dielectrics have led to extensive investigation of alternative materials with higher dielectric permittivity (high-K) in order to extend the unprecedented growth of IC complexity of the last four decades into the future.

Recently, very promising properties of epitaxially grown, crystalline rare-earth metal-oxides have been reported [1] and the integration of Pr_2O_3 dielectric in a conventional polysilicon CMOS process was successfully demonstrated [2]. However, high temperature annealing [3] and aggressive reactive ion etching (RIE) was found to degrade the initial quality of the sensitive high-K gate stack [2]. In order to minimize process induced oxide damage (PIOD), we have integrated crystalline high-K dielectrics into a virtually damage-free replacement gate process [4, 5]. For the first time, fully functional metal gate MOSFETs with crystalline Gd_2O_3 dielectric have been fabricated by means of chemical mechanical planarization (CMP) in a "gentle" damascene metal gate technology.

2. Device Fabrication

The major process steps are shown in Fig. 1. Processing is performed on 4 inch p-type Si (100) wafers. Initially, dummy gate stacks are formed by consecutive deposition, lithography and RIE (Fig. 2a), followed by self-aligned S/D ion implantation. Next, the CVD alignment-oxide is deposited and RTA anneals at 1000°C are performed to activate S/D implants. The oxide is planarized by CMP down to the gate level and the dummy gates are removed completely by wet chemical etching, leaving a self-aligned imprint of the gate stack on the Si-wafer (Fig.2b). Subsequently, crystalline Gd_2O_3 layers of 5.3 nm and 13.5 nm physical thickness are grown by molecular beam epitaxy (MBE) with smooth surface topography and good leakage currents as evident from AFM and C-AFM measurements (Fig. 4). In addition, wafers with conventional SiO_2 are fabricated as a reference. Tungsten is deposited on top of the gate dielectrics and CMP is used to pattern the damascene metal gates. Standard back-end processing completes the fabrication.

3. Results and Discussion

The fabricated devices with Gd_2O_3 gate dielectric and tungsten gate electrode (Fig. 3) are fully functional. CV measurements on Gd_2O_3 capacitors give a dielectric constant of 10.4, corresponding to EOTs of 1.9 nm and 5.1 nm respectively. Leakages are below $1 \cdot 10^{-1}$ A/cm^2 for the 1.9 nm Gd_2O_3 and $1 \cdot 10^{-3}$ A/cm^2 for the 5.1 nm, respectively, (Fig. 5), consistent with leakage requirements set by the ITRS [6].

The Gd_2O_3 gate dielectric nMOSFETs show proper transistor behavior (Fig. 6 and 7). Note that extremely low hysteresis of less than 30 mV is observed in the subVt characteristics (Fig. 7), which is a substantial improvement when compared to conventionally integrated high-K oxides [7]. In the case of process-damaged high-K oxides, large hysteresis effects with Vt-shifts of more than 300 mV have been observed which could be related to a large susceptibility to build-up charge trapping sites [7]. The subVt swing of approximately 130 mV/dec indicates high interface state densities. Charge pumping (CP) measurements revealed trap densities of $2.3 \cdot 10^{12}$ eV^{-1}cm^{-2}, consistent with the degraded subVt swing. However, only slightly reduced values of $1.8 \cdot 10^{12}$ eV^{-1}cm^{-2} are obtained for the SiO_2 reference devices which puts in question the effectiveness of the forming gas anneal when using tungsten gates. Energy resolved CP measurements on Gd_2O_3 nMOS devices showed that most of the interface traps are located in the upper half of the band gap (Fig. 8). Effective mobilities of 130 cm^2/Vs have been measured for the Gd_2O_3 MOSFETs as shown in Fig. 9. Compared to SiO_2 references this corresponds to a reduction of approx. 40% at the same effective electric field. We suspect that the acceptor-type interface states significantly degrade mobility due to Coulomb-scattering.

4. Conclusion

We have successfully integrated crystalline Gd_2O_3 with EOT of 1.9 nm in a damascene metal gate process. Since the harsh processing is done prior to high-K deposition, PIOD-effects are minimized and the initial material quality of the crystalline high-K gate dielectric is largely preserved, so that the progress in high-K material engineering can be monitored directly at the device level.

Acknowledgements

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References

[1] H. J. Osten, et al., IEDM 2001.
[2] U. Schwalke, et al., Proc. ESSDERC, p.247 (2003).
[3] S.B. Samavedam, et al., IEDM, p.307 (2003)
[4] A. Chatterjee, et al., IEDM, p.821, (1997)
[5] A. Yagishi, et al, IEDM, p.785 (1998).
[6] http://public.itrs.net/Files/2003ITRS/Home2003.htm.
[7] U. Schwalke et al, Microel. Reliab., 45, 2005.

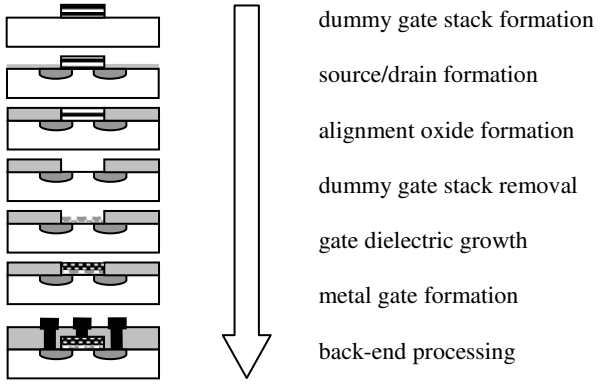

Fig. 1: Main process modules of the replacement gate technology.

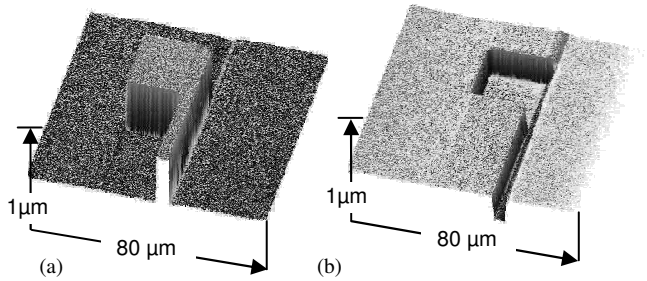

Fig. 2: Atomic force microscopy (AFM) image of a dummy gate structure (a) and a self-aligned imprint of the gate stack on the Si-substrat (b).

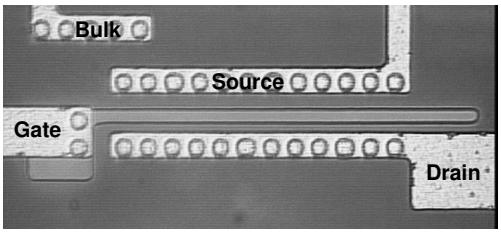

Fig. 3: nMOSFET with high-K Gd_2O_3 gate dielectric and tungsten gate electrode realized with the replacement gate process (gate length L= 4 µm and gate width W= 100 µm).

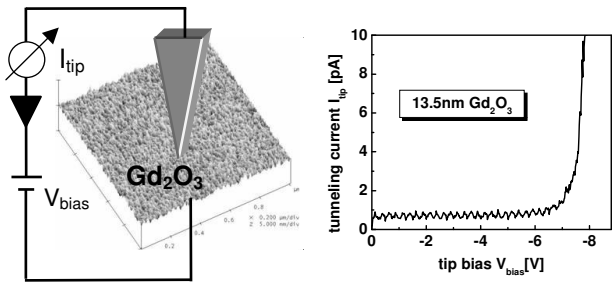

Fig. 4: Atomic force microscopy (AFM) image of the Gd_2O_3 surface (left) and nanoscale I-V sweep by conductive atomic force microscopy (C-AFM) measurement (right).

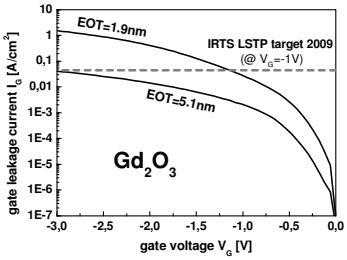

Fig 5: Gate leakage currents of 1.9 nm and 5.1 nm metal gate Gd_2O_3 pMOS capacitors (gate injection, substrate in accumulation).

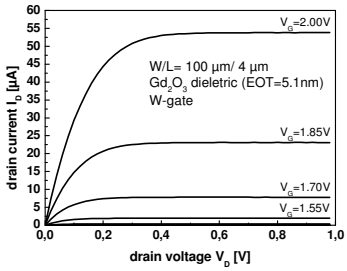

Fig. 6: Output characteristics of metal gate Gd_2O_3 nMOSFET.

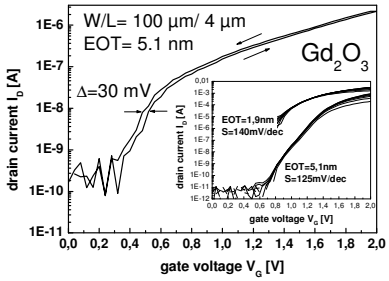

Fig. 7: Subthreshold characteristics of Gd_2O_3 nMOSFET.

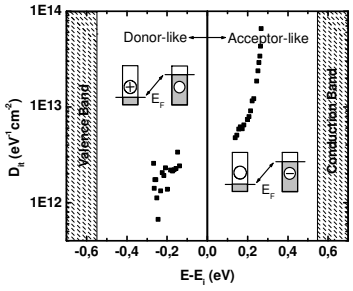

Fig. 8: Energy resolved CP measurements on Gd_2O_3 nMOS devices (EOT=5.1 nm).

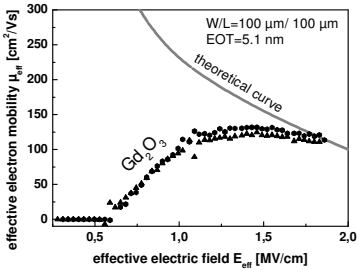

Fig. 9: Measured effective electron mobilities of damascene metal gate Gd_2O_3 nMOSFETs (EOT=5.1 nm).