Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 416-417

P-1-8

Investigation of Inversion C-V Reconstruction for Long-Channel MOSFETs with Leaky Dielectrics using Intrinsic Input Resistance Approach

Wei Lee, Pin Su, *Ke-Wei Su, *Chung-Shi Chiang, *Sally Liu
Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan (e-mail: pinsu@mail.nctu.edu.tw)
*Taiwan Semiconductor Manufacturing Company, 9, Creation Rd. 1, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C.

1. INTRODUCTION

The gate capacitance-voltage (C-V) characteristic is fundamental to CMOS technology development because it plays an important role in oxide thickness extraction, carrier mobility calculation, interface trap characterization, and so on. As the gate dielectric thickness is reduced (below 20 Å), the inversion C-V characteristic is distorted due to direct tunneling current. Although Goo *et al*. [1] demonstrated that the conventional two-element parallel model (Fig. 1(a)) can provide valid C-V characteristics for short-channel devices (e.g., below 0.2 μm [1]), using these devices in C-V measurement has several drawbacks such as small intrinsic capacitance, large parasitic components (Fig. 2) and uncertainty in the physical gate length. In other words, the variation of measured C-V increases as channel length decreases (Fig .3). Therefore, the C-V reconstruction for long-channel MOSFETs is still a crucial issue.

Several studies have constructed the C-V characteristic for long-channel devices using distributed circuit approaches [2]-[4]. For example, Barlage *et al*. [2] proposed using a transmission line concept to extract the inversion MOS capacitance. In [4] we employed segmented SPICE simulation (Fig. 4(a)) with each sub-transistor modeled by the BSIM4 MOSFET model to simulate the anomalous C-V characteristics due to gate direct tunneling (Fig. 4(b) and (c)). Although these methods may provide well-restored characteristics, the implementation is too complicated to be routinely used in a technology development.

To develop a simple method for the inversion C-V reconstruction, the challenge lies in capturing the distributed nature of the gate capacitance and the channel resistance in a compact way. This is analogous to the gate input impedance modeling in the compact model development for RF CMOS, where an intrinsic input resistance has been introduced [5] as a major part of the gate input resistance. This paper presents an inversion C-V reconstruction method for long-channel MOSFETs using the concept of intrinsic input resistance.

2. METHOD

Fig. 5(a) shows BSIM4/SPICE-simulated C-V characteristics for devices with leaky dielectric. Segmented SPICE simulation that divides the transistor along the length direction with 10 sub-transistors in series (Fig. 5(b)) was utilized and the BSIM4 device model parameters were well calibrated as described in [4]. As shown in Fig. 5(a), a substantial attenuation in the inversion capacitance for long-channel MOSFETs can be seen. The attenuation results mainly from the gate tunneling induced de-biasing effect. Also shown in Fig. 5(a) is that a single transistor simulation with an intrinsic input resistance, R_{ii}, added to the gate terminal in addition to gate electrode resistance (Fig. 5(c)) yields nearly identical results as those of segmented simulation.

R_{ii} represents a channel-reflected gate resistance and can be thought of as an equivalent resistance accounting for the first-order non-quasi-static effect in the channel [5][6]. R_{ii} is proportional to the total channel resistance with a proportional constant α, which accounts for the distributed effect of the complex RC network constructed by the gate capacitance and the channel resistance. Since this RC network has a short termination at both source and drain nodes in the C-V measurement, α can be approximated as 1/12 because the location at which the gate current equals zero occurs at L/2 [6]. The channel resistance has been modeled in BSIM4 [5][6] and may be extracted from the measured I-V (i.e., $(dI_{ds}/dV_{ds})^{-1}$). Fig. 6 shows that R_{ii} dominates the total gate resistance for the device with long channel length (L = 10 μm) and therefore is crucial in the C-V reconstruction of long-channel MOSFETs.

As indicated in Fig. 5(a), the concept of intrinsic input resistance can be used to develop a simple method for the inversion capacitance extraction. As the conventional three-element model (Fig. 1(b)) is used to represent the small-signal equivalent model of a leaky MOS capacitor, the total series resistance, R_s, can be calculated by $R_{ii} + R_{ge} + R_{sd}/2$. The inversion C-V may then be reconstructed by [3][7]:

$$C_{OX} = C_m \Big/ ((1 - G_m R_s)^2 + \omega^2 C_m{}^2 R_s{}^2) \quad (1)$$

where C_m and G_m represent the measured capacitance and conductance, respectively, using the parallel circuit model of the LCR meter (Fig. 1(a)).

3. MEASUREMENT AND RESULTS

Standard MOSFETs with doped poly-Si gate electrode were fabricated and tested in this study. The EOT is about 11 Å. The impedance analyzer HP4294A was used in the C-V measurement. The measurement frequency is 1 MHz. Fig. 7(a) and Fig. 7(b) show the measured inversion capacitance and our reconstructed C-V characteristics for NMOS and PMOS, respectively. The impact of R_{ii} on the reconstructed results can be seen. Moreover, the correction for PMOS is larger because the lower PMOS channel mobility may result in a higher channel resistance and R_{ii}. Besides, the reconstructed C-V characteristics show a slight decrease in the high V_{GS} regime. This may be attributed to poly-depletion effects. Also shown in Fig. 7 are the theoretical characteristics provided by the NCSU CVC (C-V analysis software developed by the North Carolina State University) [8][9]. Our reconstructed C-V curves agree with the NCSU-CVC simulation results.

4. CONCLUSIONS

We present an inversion C-V reconstruction method for long-channel MOSFETs using the concept of intrinsic input resistance. The concept has been validated by segmented BSIM4/SPICE simulation. Our reconstructed C-V characteristics show poly-depletion effects and agree with the NCSU-CVC simulation results. Due to its simplicity, this method can be used for regular process monitoring purposes.

ACKNOWLEDGEMENT

This work was supported in part by the National Science Council of Taiwan under contract NSC94-2215-E-009-049.

REFERENCES

[1] J.-S. Goo et al., *IEEE EDL*, **25**(12), 2004
[2] D. W. Barlag et al., *IEEE EDL*, **21**(9), 2000
[3] C.-H. Choi et al., *IEEE TED*, **47**(10), 2000
[4] W. Lee et al., *IEEE VLSI TSA*, 2005
[5] X. Jin et al., *IEDM*, 1998
[6] W. Liu, "MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4", John Wiley & Sons, 2001
[7] E. M. Vogel et al., *IEEE TED*, **47**(3), 2000
[8] J. R. Hauser et al., *Proc. AIP Int. Conf. Characterization Metrology ULSI Technology*, Gaithersburg, MD, 1998
[9] W. K. Henson et al. *IEEE EDL*, **20**(4), 1999

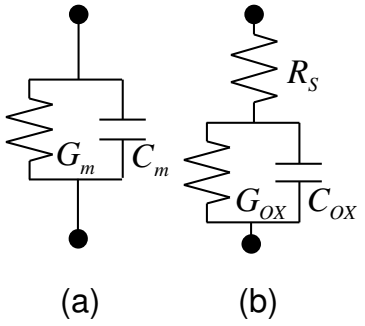


Fig. 1. Small-signal equivalent models for MOS capacitor. (a) Two-element parallel model. (b) Three-element model.

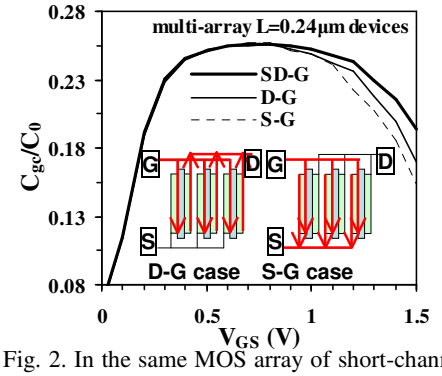


Fig. 2. In the same MOS array of short-channel devices, the impact of on-chip inductance (L_i) depends on the measurement configuration. C_{gc} : inversion capacitance. C_0 : true capacitance for L = 10 μm.

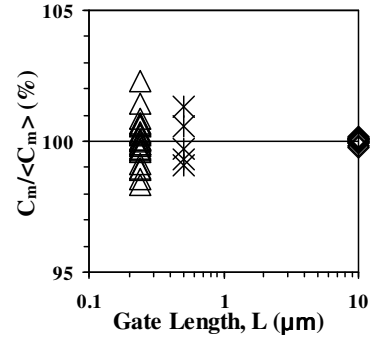
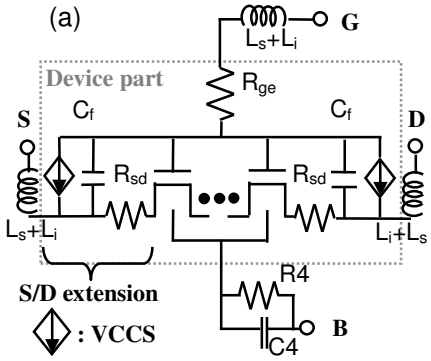
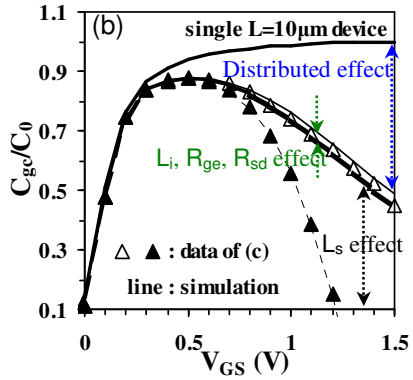


Fig. 3. The variation of C_m increases as L decreases. C_m : measured capacitance.





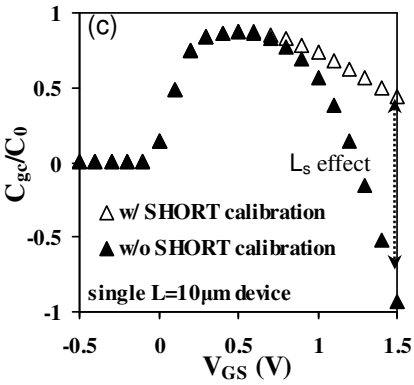
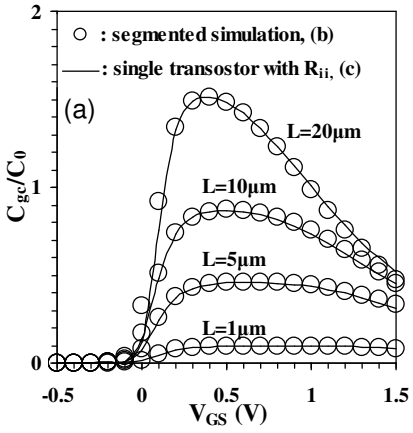


Fig. 4. BSIM4-based macro model to simulate the anomalous C-V characteristics caused by gate direct tunneling [4]. R_{ge} : gate electrode resistance. R_{sd} : source/drain resistance. L_s : cable inductance. C_f : fringing capacitance. R4 = 1e9 Ω, C4 = 1e-9 F.



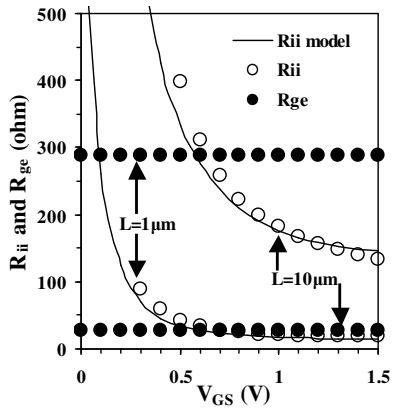


Fig. 6. R_{ii} and R_{ge} versus V_{GS} for devices with L = 1 μm and 10 μm. (Symbols : extracted date. Lines : model)

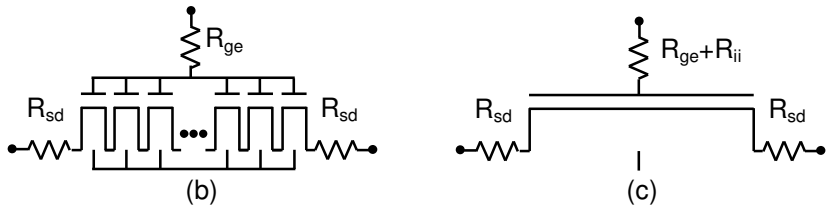
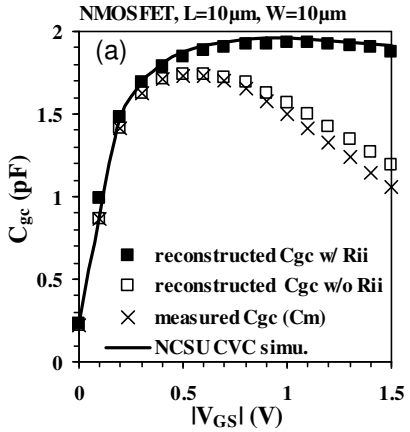


Fig. 5. (a) The gate-tunneling induced C-V attenuation can be simulated by BSIM4/SPICE simulation. (b) Segmented SPICE simulation with each sub-transistor modeled by the BSIM4 MOSFET model. (c) Single transistor SPICE simulation with R_{ii} added to the gate terminal in addition to R_{ge}. R_{ge} : gate electrode resistance. R_{sd} : source/drain resistance.



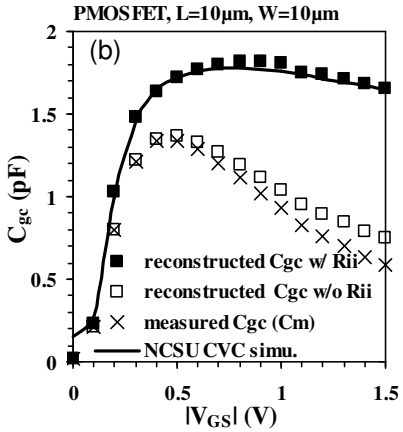


Fig. 7. Reconstructed C-V characteristics for (a) NMOS and (b) PMOS with and without considering R_{ii}. The results agree well with the simulation results of NCSU CVC [8][9]. (T_{OX} = 1.15 nm. NMOS : N_{Bulk} = 3E17 cm^{-3}, N_{Gate} = 1.8E20 cm^{-3}. PMOS : N_{Bulk} = 2.5E17 cm^{-3}, N_{Gate} = 8.5E19 cm^{-3}.)