Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 766-767

P-10-13

Fabrication of Nano-gate Structure Organic Static Induction Transistor using Electron Beam Lithography

Masaharu Fukuda[1], Hiroshi Yamauchi[1], Masaaki Iizuka[2] and Kazuhiro Kudo[1]

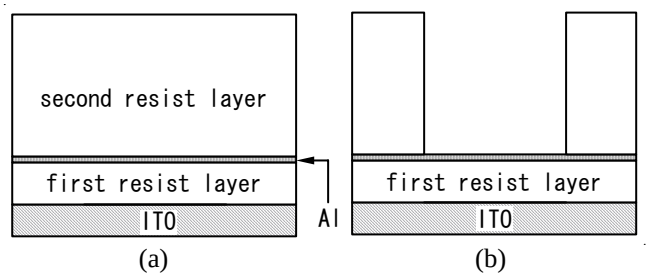
[1]Department of Electronic and Mechanical Engineering, Faculty, Chiba University
[2]Faculty of Education, Chiba University
1-33 Yayoi-cho, Inage-ku, Chiba 263-8522, Japan
Phone: +81-43-290-3324
E-mail: masaharu.f@graduate.chiba-u.jp

1. Introduction

Optoelectronic elements using organic materials show promise for low-cost, large-area and flexible devices. Conventional field effect transistors (FETs) using organic materials have low-speed, low-power and relatively high operational voltage mainly due to their low-mobility and high-resistivity. It is known that the static induction transistor (SIT) is a promising device because of the high-speed and high-power operation. The excellent characteristics of the SIT mainly arise from vertical structure with a very short distance between the source, drain and gate electrodes [1,2]. The static characteristics demonstrate that the majority carriers of hole in the organic material flow from the source to drain and controlled by the gate voltage applied to the Schottky gate electrode.In this case, drain-source current (I_{DS}) is restricted by spreading the depletion layer around the Schottky gate electrode under the gate voltage (V_G)

The characteristic of SIT depends on the distance between the source-gate, gate-source and gate electrode gap. Therefore we tried to fabricate organic SIT having nano-gate structure by electron beam exposure and Reactive Ion Etching (RIE). This process can control and fabricate fine gate electrode and the distance of gate gaps. Inserting the resist film of between the source and gate electrode as the insulator, reduces a gate leakage current. The fabrication process used here is simple to control the film thickness of resist, and organic layer, and the distance between source and gate, gate and drain electrode. The purpose of this study is the improvement of SIT characteristic by optimizing the gate structure, using the process mentioned above and device simulation.

2. Experimental details



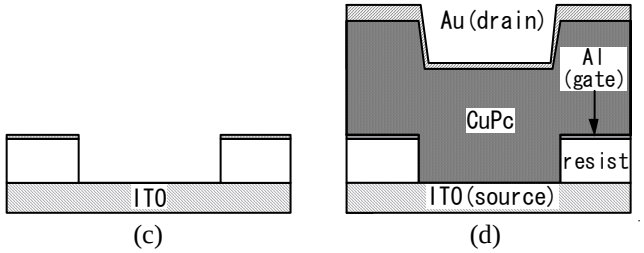


Fig.1 Fabrication process of organic SIT. (a) Fabrication of Al and resist layer. (b) Expose the second resist layer using electron beam exposure, and lift-off. (c) Al and first resist layer etching by RIE. (d) CuPc and Au layer were deposited.

Fig.1 shows the fabrication process of organic SIT. The first resist layer (150 nm) spin coated on indium-tin-oxide (ITO) coated glass substrate. Then, gate electrodes (Al: 15 nm) were evaporated on the first resist layer, and the second resist layer (400 nm) spin coated on the Al layer. (Fig.1 (a)). Second resist layer was patterned using electron beam exposure. After the lift-off process (Fig.1 (b)), second resist layer use the etching mask of Al and first resist layer.(Fig.1(c)). CuPc film (370 nm) was deposited on this patterned substrate. Finally, drain electrodes (Au: 60 nm) were formed by vacuum evaporation (Fig.1 (d)).

3. Results and discussion

. First, we evaluated the insulating characteristic of resist film. Fig.2 shows the device structure and electrical characteristic of resist in the range of driving current level of typical SIT. Fig.2 shows that the resist film used here high insulating properties in the range of SIT operation.

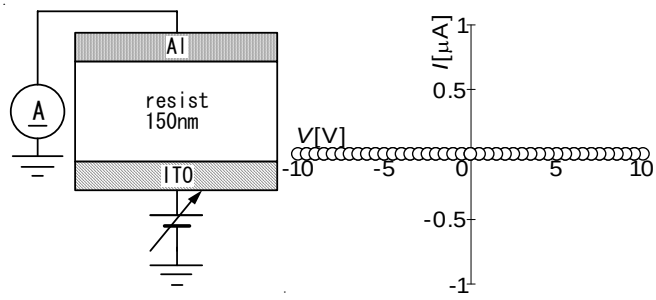


Fig.2 Device structure and insulative characteristic of resist layer.

Second, we investigated the etching rate of Al and second resist layer of RIE. Cl_2 gas was used to etch the Al

layer, and O_2 gas was used to etch the first resist layer. Fig.3 (a) shows the etching rate of Al and resist layer in the Cl_2 gas at the room temperature, (b) shows the etching rate of Al layer depend on the substrate temperature. At room temperature, Al and resist etching ratio (resist/Al) is over 100. Etching rate is increase according to the substrate temperature from 20℃ to 40℃. In this study adopt the substrate temperature was fixed at 40℃. Fig.4 shows the SEM image of gate electrode surface. Gate electrode edge have concavity and convexity, by reason that after corrosion of Al and fabricated the conductive film on the whole area of substrate to use SEM.

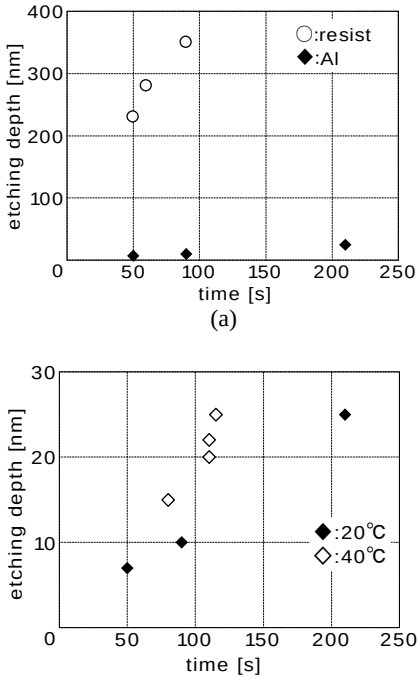


Fig.3 Etching rate of Al and resist layer. (a) Etching ratio of Al and resist layer in the Cl_2 gas at the room temperature. (b) Etching rate of Al layer depend on the substrate temperature.

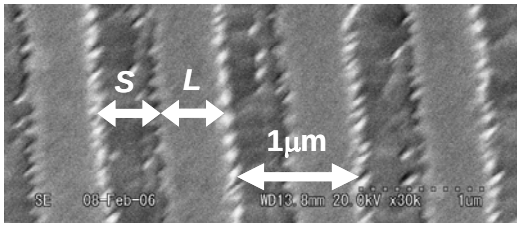


Fig.4 SEM image of gate electrode surface. *L* is gate electrode width, *S* is gate electrode gap. (*L*/*S*=500/500 nm)

Fig.5 shows the static characteristic of SIT. I_{DS} at a constant V_{DS} decrease with increasing V_G. Although, ON current is sufficiency to driving organic electroluminescence device, OFF current is rather large. This large OFF current is mainly due to the wider gate gap comparing the spreading depletion layer between gate electrodes. It is necessary to optimize the structure and the carrier density of organic semiconductor to improve the characteristic of organic SIT.

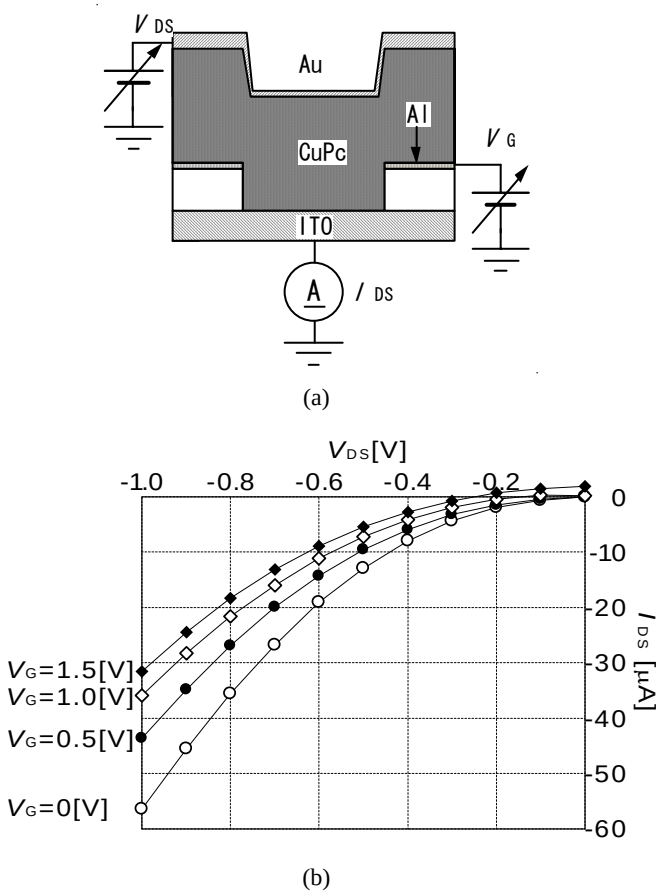


Fig.5 Static characteristic of the organic SIT. (a) Device structure of the organic SIT and the electrical measurement system for static characteristic. (b) Static I_{DS}-V_{DS} characteristic of the organic SIT.

3. Conclusions

We have fabricated organic SIT with nano-gate structure using electron beam exposure and RIE., and show the basic operation of the organic SIT. Although off current is very high, it is expected that the device properties can be improved by optimizing the device structure and choosing proper organic materials.

References

[1] Kazuhiro Kudo, Satoshi Tanaka, Masaaki Iizuka, Masakazu Nakamura, Thin Solid Films 438-438 (2001) 330-333

[2] Kazuhiro Kudo, Dong Xing Wang, Masaaki Iizuka, Shigekazu Kuniyoshi, Kuniaki Tanaka, Thin Solid Films 331 (1998) 51-54

[3].Y.Tanaka, D.X.Wang, M.Iizuka, S.Kuniyoshi, K.Kudo, K.Tanaka, TECHNICAL REPORT OF IEICE OME98-78 (1998-09)