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High-Quality-Factor and Low-Power-Loss Micromachined RF Bifilar Transformer for UWB RFIC Applications

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In this paper, we demonstrate that high-quality-factor and low-power-loss transformers can be obtained by using the CMOS process compatible backside inductively-coupled-plasma (ICP) deep trench technology to selectively remove the silicon underneath the transformers. A 20.6 dB and a 16.3 dB improvement in isolation (S_{21}) were achieved at 5.2 GHz and 10 GHz, respectively, for a dummy open device for pad de-embedding after the backside ICP dry etching. A 62.4% and a 205.8% increase in Q-factor, and a 10.3% and a 30.2% increase in maximum available power gain (G_{Amax}) were achieved at 5.2 and 10 GHz, respectively, for a bifilar transformer with overall dimension of 240 μm × 240 μm after the backside ICP etching. The G_{Amax} of 0.769 (at 5.2 GHz) and 0.849 (at 10 GHz) are both state-of-the-art results among all reported on-chip bifilar transformers. These results show the backside ICP deep trench technology is very promising for RFIC applications.

Fig. 1(a) shows the top-view die photo of the symmetrical bifilar transformer under study, which has turn number of 2, metal width of 10 μm, coil spacing (between the primary and the secondary coil) of 5 μm, inner dimension of 100 μm × 130 μm, and overall dimension of 240 μm × 240 μm. What is also shown in Fig. 1(a) is a typical backside die photo of a transformer after the ICP etching. Port-1 and Port-2 stand for the input port and the output port of the network analyzer. The transformer was fabricated with a 0.18 μm RF-CMOS technology on a p-type silicon substrate with thickness of 300 μm and resistivity of 10 Ω-cm. The main features of the backend processes are as follows. There are 6 metal layers. We name the metal layers M1 to M6 from the bottom to the top. The thickness of M6 is 0.99 μm, and the others is 0.53 μm. The oxide thickness between M6 and M5, between other adjacent metal layers, and between M1 and the silicon substrate are 1 μm, 0.85 μm, and 1.1 μm, respectively. The processing steps of our backside ICP deep trench technology are shown in Fig. 1(b) and described as follows. After standard photolithography processes on the backside of the die, the ICP etching (etching rate ≈ 2 μm/min) was used to remove the silicon underneath the transformers. The main gases used during the ICP etching process were alternate SF_6 (for etching) and C_4F_8 (for passivation) with a 17-second cycle. Finally, the adhesive and photoresist, which covered the front-side and backside of the die respectively, was removed for test purpose.

The frequency-dependent S-parameter measurements were performed by an Agilent 8510C network analyzer. The expressions of the G_{Amax}, Q factors (Q_1 and Q_2), magnetic-coupling factor (k_{Im}), and resistive coupling factor (k_{Re}) of an transformer in terms of its measured Z-parameters, which can be converted from the measured S-parameters, can be found in Ref. [1]. A 20.6 dB (from -40.4 dB to -61dB) and a 16.3 dB (from -38.7 dB to -55 dB) improvement in isolation (S_{21}) were achieved at 5.2 GHz and 10 GHz, respectively, for a dummy open device (for pad de-embedding) after the backside ICP etching, as shown in Fig. 2(a). The improvement in isolation is mainly due to the reduction of the parasitic capacitance through the substrate achieved by the substrate etching. What is also shown in Fig. 2(a) are the measured Q_1 versus frequency characteristics of the bifilar transformer. A 62.4% (from 8.99 to 14.6) and a 205.8% (from 8.6 to 26.3) increase in Q-factor were achieved at 5.2 and 10 GHz, respectively, for the bifilar transformer after the backside ICP etching.

Fig. 2(b) shows the measured k_{Im}, k_{Re} and G_{Amax} versus frequency characteristics of the bifilar transformer. The influence of the ICP etching on k_{Im} is very small because it mainly depends on the geometry of the coils. Very low k_{Re} smaller than 0.01, i.e. nearly pure magnetic-coupling, was achieved for frequencies up to 5.7 GHz for the bifilar transformer after the backside ICP etching. This is reasonable because the coupling between the primary and the secondary coil should be predominately inductive if the substrate under the transformer is etched away. A 10.3% (from 0.697 to 0.769) and a 30.2% (from 0.652 to 0.849) increase in G_{Amax} were achieved at 5.2 and 10 GHz, respectively, for the bifilar transformer after the backside ICP etching. Because the measured G_{Amax} of the ICP transformer is high enough (0.686 – 0.843) in the 3.1-10.6 GHz band, it is very suitable for 3.1-10.6 GHz ultra-wideband (UWB) applications [2]. Table I shows a detailed comparison of the extracted parameters of the bifilar transformer in this work, and the bifilar transformers in [1] and [3]. The G_{Amax} of 0.769 (5.2 GHz) and 0.849 (10 GHz) in this wok are better than those (0.764 and 0.687) of the bifilar transformer on porous silicon with overall dimension of 280 μm × 280 μm [3], and better than those (0.603 and 0.653) of the bifilar transformer on a quartz substrate with overall dimension of 300 μm × 300 μm [1]. Moreover, the simulated results show that if the backside ICP etching in conjunction with a thick top metal of 3.02 μm (i.e. the top metal thickness in [3]) is adopted, then very high Q-factors (Q_1 and Q_2) about 70 and G_{Amax} about 0.94 can be achieved (not shown here).

REFERENCES

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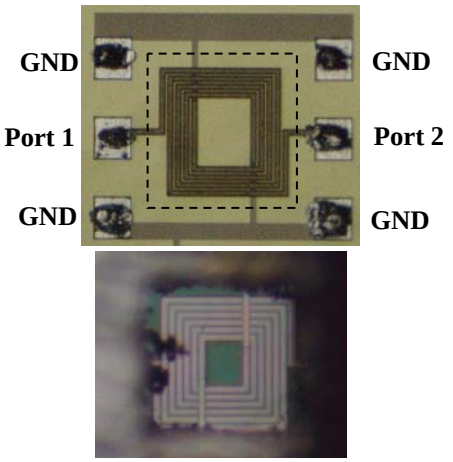
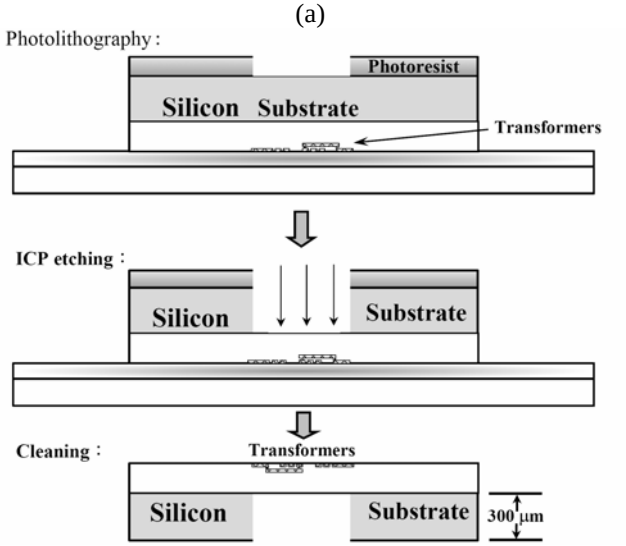
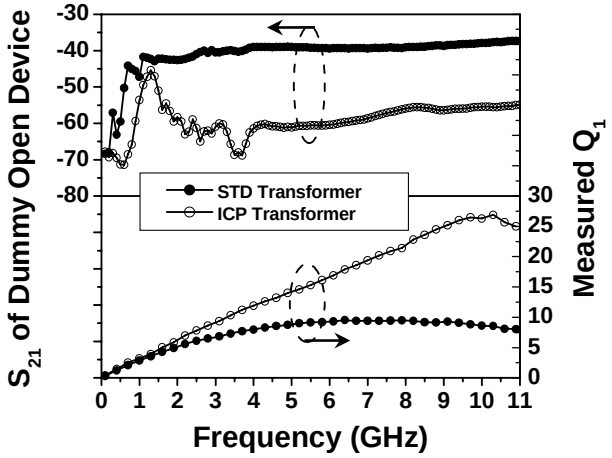


(a)

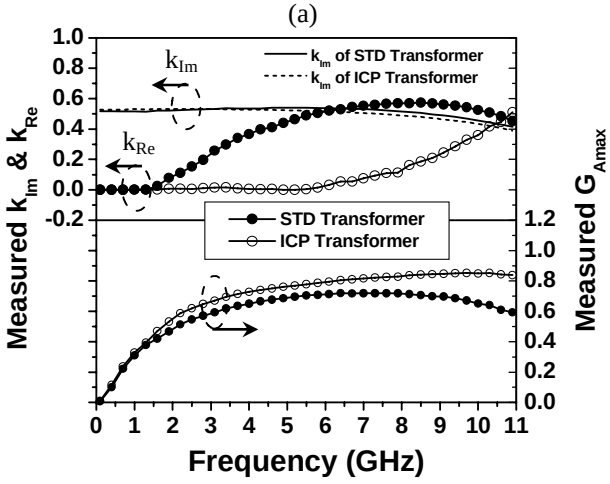


(b)

Fig. 1 (a) Top-view die photo of the transformer under study. Typical backside die photo of a transformer after backside ICP etching is also shown. (b) Process steps of the backside ICP deep trench etching technology.



(a)



(b)

Fig. 2 Measured (a) Q_1 versus frequency characteristics, and (b) k_{Im}, k_{Re}, and G_{Amax} versus frequency characteristics of the bifilar transformer before and after the backside ICP dry etching. Measured S_{21} characteristics of a dummy open pad device are also shown in (a).

Table I A detailed comparison of the extracted parameters between the bifilar transformer in this work, and the bifilar transformers in [1] and [3].

	Transformer Structure	Overall Dimension (μm^2)	Technology	substrate resistivity (Ω·cm)	frequency (GHz)	Q_1	Q_2	k_{IM}	k_{Re}	x	G_{Amax}
K. Chong [3]	Thick (3.02 μm) Bifilar (on porous Si substrate)	280×280	NA	NA	5.2	9.1	9.1	0.75	0.38	1.83×10^{-2}	0.764
					8	6.69	6.69	0.825	0.665	1.81×10^{-2}	0.765
					10	2.36	2.36	0.9	0.9	3.58×10^{-2}	0.687
K. T. Ng [1]	Thin (0.85 μm) Bifilar (on normal Si substrate)	300×300	NA	10	5.2	2.857	2.619	0.623	0.6	1.96×10^{-1}	0.424
					8	1.619	1.333	0.589	0.762	3.16×10^{-1}	0.342
					10	1	0.571	0.43	0.73	7.3×10^{-1}	0.213
	Thin (0.85 μm) (on quartz substrate)			∞	5.2	6.143	6.524	0.608	0.169	6.55×10^{-2}	0.603
					8	7.619	8.143	0.589	0.139	4.55×10^{-2}	0.655
					10	8	8.429	0.565	0.1	4.6×10^{-2}	0.653
This Work	Thin (0.99 μm) Bifilar (on normal Si substrate)	240×240	0.18 μm CMOS	10	5.2	8.99	8.9	0.54	0.464	3.3×10^{-2}	0.697
					8	9.44	9.34	0.515	0.571	2.81×10^{-2}	0.716
					10	8.6	8.49	0.456	0.525	4.63×10^{-2}	0.652
	Thin (0.99 μm) Bifilar (w/i backside ICP etching)				5.2	14.6	14.5	0.523	3.5×10^{-4}	1.73×10^{-2}	0.769
					8	21.7	21.6	0.489	0.122	8.77×10^{-3}	0.829
					10	26.3	26.2	0.433	0.36	6.7×10^{-3}	0.849