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Sub-Atmospheric Chemical Vapor Deposition Process for Chip-to-Wafer 3-Dimensional Integration

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1. Introduction

In recent years, three-dimensional (3D) integration for high performance LSI has attracted much attention since this technology can solve interconnection problems by the use of Si-through vertical interconnections between stacked LSI chips. The 3D LSI has great advantages such as short wire length, high packaging density, high-speed operation, low power consumption, and high feasibility for parallel processing. We have previously fabricated 3D LSI based on wafer-to-wafer or chip-to-wafer bonding technologies [1-4].

The formation process of vertical buried interconnections through a Si substrate consists of deep-Si-trench etching, dielectric layer formation along the high-aspect-ratio Si trench, and trench filling with conductive materials. A low-temperature process below 400 °C is strongly required for the vertical interconnection formation to avoid the heat damage to MOSFET or metal wiring in LSI chips.

In this paper, we describe a sub-atmospheric chemical vapor deposition for chip-to-wafer 3D integration technology to form dielectric layer of SiO_2 with high step coverage at low temperature.

2. Chip-to-wafer 3D integration technology

Figure 1 conceptually shows cross-sectional structure of 3D LSI fabricated using chip-to-wafer 3D integration technology. In this figure, two completed LSI chips are vertically stacked on a supporting LSI wafer. The respective layers in 3D LSI are electrically connected by a number of vertical interconnections composed of buried interconnections and metal microbumps.

The fabrication sequence for chip-to-wafer 3D integration technology is shown in Fig. 2. After LSI wafer testing, the wafer is diced into many LSI chips. Defective dies are selectively removed in the following sorting process to obtain many Known-good-dies (KGDs). After that, the KGDs are temporally glued onto a handling substrate using photoresist as adhesive. Then, buried interconnections and metal microbumps are formed in the KGDs. Finally, the KGDs with vertical interconnections are stacked on the supporting LSI wafer. In this chip-to-wafer 3D integration, buried interconnections are formed after the formation of both MOSFET and metal wiring.

3. Sub-atmospheric chemical vapor deposition for SiO_2 formation on deep Si trenches

We have previously formed buried interconnections filled with phosphorus-doped polycrystalline silicon (poly-Si) or tungsten as conductive materials. Thermal SiO_2 film was employed for the insulator between buried interconnections and the Si substrate. However, thermal oxidation is not suitable for the buried interconnection formation in our chip-to-wafer 3D integration due to its high-temperature process. Although plasma enhanced chemical vapor deposition (PECVD) and atmospheric pressure chemical vapor deposition (APCVD) are widely used as low-temperature process for dielectric film formation, these processes have a serious disadvantage of low step coverage. To solve this problem, sub-atmospheric chemical vapor deposition (SACVD) with a tetraethylorthosilicate (TEOS)/O_3 gas system is applied for the formation of SiO_2 layer in deep Si trench. In this system, gas-phase reaction occurs to afford reactive precursors such as Si-O or Si-OH, and SiO_2 is finally generated by surface reactions such as Si-OH elimination and Si-O incorporation into bulk film [5]. Therefore, SiO_2 film with high step coverage can be obtained by the SACVD process, compared with the PECVD and APCVD process.

4. Experimental results and discussion

The schematic diagram of TEOS/O_3 reactor is shown in Fig. 3. TEOS was carried with He gas, and both N_2 and O_2 gases were used as dilution gases and a reactor was vacuumed by dry pump. An ozonizer generates O_3 from O_2 gas by silent discharge. The reactor pressure was ranging from 15 to 30 kPa and the substrate temperature was set at around 300-400 °C.

The relationships between step coverage and reactor pressure during SiO_2 deposition by SACVD are shown in Fig. 4. The step coverage is a ratio of the bottom SiO_2 thickness to the top SiO_2 of the trench. The trench with a depth of 35 μm and a surface dimension of 3-μm square were etched by the Bosch process. The step coverage increased by raising the reactor pressure. It is considered that a high reactor pressure promotes the surface reaction since a large amount of dilution gas to obtain high reactor pressure decreased the partial pressure of TEOS and O_3. The SEM micrographs of SiO_2 film deposited on the deep-Si trench at 350℃ are shown in Fig. 5. As seen in the figure, more than 60% of step coverage was obtained in this SiO_2 deposition. Figure 6 also shows SEM micrographs of SiO_2 film formed by SACVD on the deep-Si trench with 7-μm-thick SiO_2 passivation layer by PECVD. The Si trench through SiO_2 layer was formed by the Bosch process after SiO_2 etching and protection film formation on the sidewall of SiO_2 hole to reduce excess side etching of Si at the interface between SiO_2 and Si substrate [6]. The SiO_2 layer with a thickness of more than 300 nm is uniformly deposited on both the sidewall and the bottom of the deep trench. Overhang or bowing were hardly observed, as seen in this figure.

The electrical properties of the resultant SiO_2 film are very important factors for our 3D integration technology. Figure 7 shows the capacitance-voltage (*C-V*) characteristics and current-voltage (*I-V*) characteristics of the SiO_2 film deposited by SACVD with TEOS/O_3. Compared with SiO_2 films formed by thermal oxidation or PECVD, electrical leakage of the SiO_2 films formed by SACVD is relatively high. However, leakage current of the SiO_2 films can be reduced by increasing film thickness or improving film quality.

5. Conclusion

The SACVD with TEOS/O_3 gas system was introduced for low-temperature SiO_2 deposition in chip-to-wafer 3D integration technology. We have successfully formed SiO_2 film with high step coverage of more than 60% on both the sidewall and bottom of deep-Si trench at 350℃. This result shows that the SACVD process with TEOS/O_3 gas system is suitable for our chip-to-wafer 3D integration technology.

Acknowledgments

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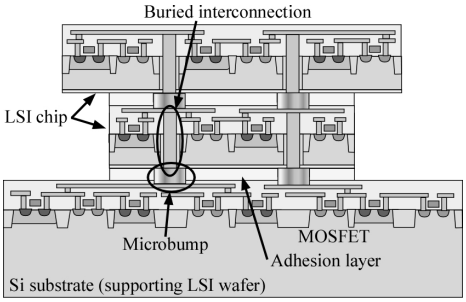


Fig. 1. Cross-sectional structure of 3D LSI fabricated using chip-to-wafer 3D integration technology.

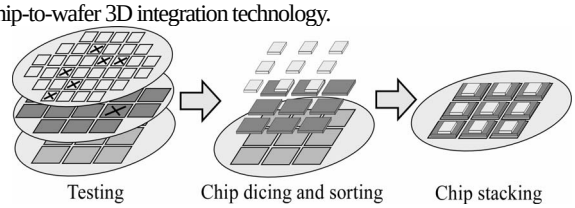


Fig. 2. Fabrication sequence for chip-to-wafer 3D integration technology.

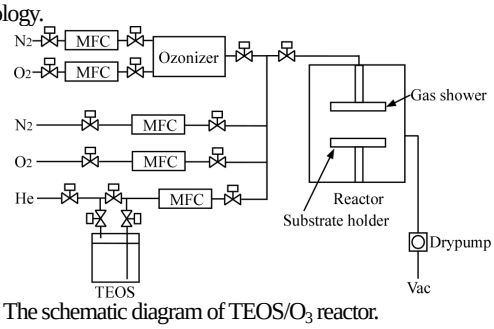


Fig. 3. The schematic diagram of TEOS/O_3 reactor.

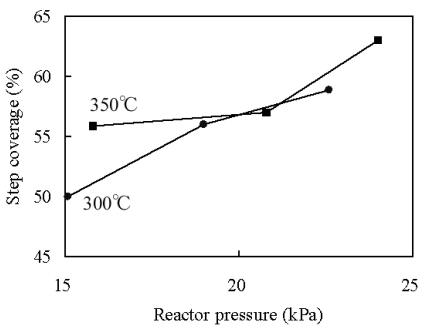


Fig. 4. Relationships between reactor pressure and step coverage of SiO_2 deposition in deep Si trench.

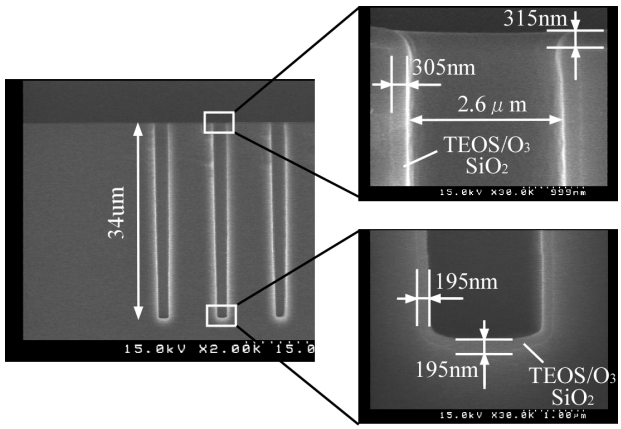


Fig. 5. SEM cross-sectional view of SiO_2 film formed by SACVD on the deep Si trench.

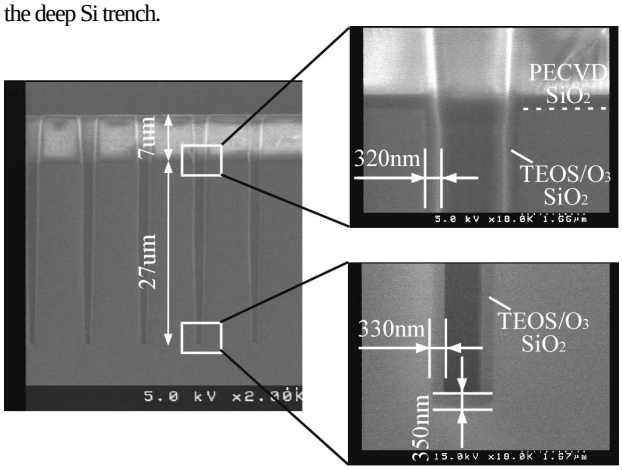
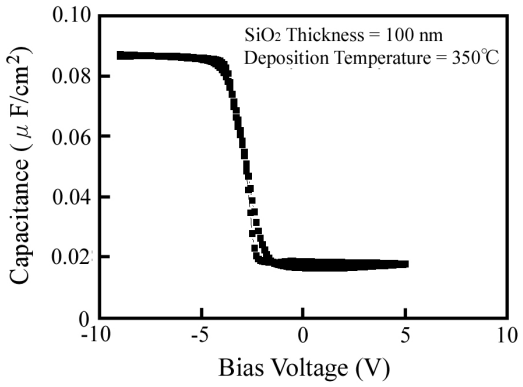
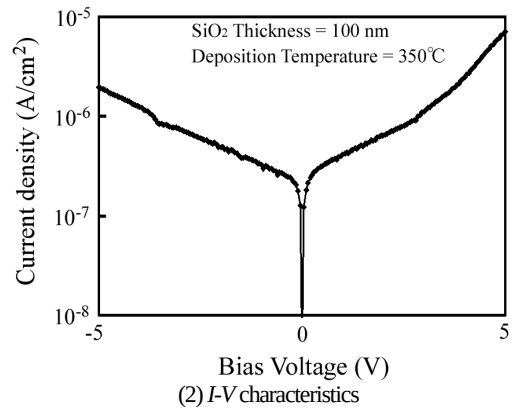


Fig. 6. SEM cross-sectional view of SiO_2 film formed by SACVD on deep Si trench with thick passivation layer.



(1) *C-V* characteristics



(2) *I-V* characteristics

Fig. 7. *C-V* and *I-V* characteristics of SiO_2 film deposited by SACVD with TEOS/O_3