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Impacts of Layout Dimensions and Ambient Temperatures on Silicon Based On-Chip RF Interconnects

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Abstracts

In this paper, we present the systematic analysis of on-chip interconnects for deep sub-micron silicon-based RFIC applications, including the impacts of layout dimensions (signal line width and spacing between signal line and grounding line) and ambient temperatures. The frequency depended RLGC elements in infinity small subsection were extracted from measured S-parameters and with traditional Telegrapher's RLGC model. We find that not only their own layout dimensions but also ambient temperature strongly affect the frequency depended RLGC elements.

1. Introductions

Recently, following prompt increase of operating frequency, the silicon-based interconnects, which are laid between modules in system-on-chip (SOC), have attracted many attentions for radio frequency integrated circuits (RFICs) and the long interconnects must be treated as transmission lines. Thus, it is usual to use frequency depended Telegrapher's RLGC model to characterize the RF performances of interconnects, and many RLGC extraction methodologies from the measured scatter parameters matrixes have been developed [1][2]. Furthermore, for accurately measuring, interconnects are usually laid with one signal line on the center and two grounding lines on two sides to provide good shielding. Besides, we remove the center signal line but keep the grounding lines on two sides as the open structure. Many papers have put more emphasis on the influences of signal line width [3][4]; however, even for the same signal line width, we found the spacing between signal lines and grounding lines would affect the RLGC parameters significantly due to skin effect and proximity effect. Additionally, ambient temperature would also result in series resistances changes of interconnects. In this work, we investigate RF interconnects' characteristics as a function of layout dimensions under various ambient temperatures in detail. The results are important for modeling interconnects in advanced high frequency circuits in which the spacing is smaller.

2. Experiments

As shown in Fig. 1 (a), the interconnect samples for this study composed one signal line and two grounding lines on two sides were prepared by 90 nm CMOS process technology. The width of center signal line and two grounding lines are 2 um or 15 um and 100 um, respectively. The length of signal line and grounding line are all 500 um and spacing between them is 2 um or 15 um. These interconnects were laid on metal 7 without any metal below them. Three different ambient temperatures of -25°C (LT), 25 °C (RT), and 125°C (HT) were set to observe the temperature effects. In addition, Agilent 8510 VNA with the frequency up to 30 GHz and Agilent 4156 for DC source were employed for scatter parameters measurements. Prior to scatter parameters measurements, methods of Short-Open-Load-Thru (SOLT) were used for calibration at each temperature to correct for temperature variation in the system [5]. Additionally, open dummy structures, which remove the center signal line but keep the grounding lines on two sides as shown in Fig. 1 (b), were used for accurate de-embedding.

3. Results and Discussions

With traditional Telegrapher's RLGC model, propagation constant γ and line impedance Z could be derived directly from de-embedded measured scatter parameters as follows [1]:

$$e^{-\gamma l} = \left(\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right)^{-1} \quad (1)$$

$$K = \left\{ \frac{\left(S_{11}^2 - S_{21}^2 + 1\right)^2 - 4S_{11}^2}{4S_{21}^2} \right\}^{0.5} \quad (2)$$

$$Z^2 = Z_0^2 \frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2} \quad (3)$$

Where Z_0=50Ω, ***l*** was the length of interconnect. S_{ij} (i,j=1,2) were the measured scatter parameters after de-embedding. Due to the relations of $Z = \sqrt{(R + j\omega L)/(G + j\omega C)}$ and $\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$, the frequency depended parameters per unit length in infinitely small subsections, shown in Fig. 2, could be derived as follows:

$$R(f) = \mathrm{Re}(\gamma Z) \quad (4)$$

$$L(f) = \mathrm{Im}(\gamma Z)/2\pi f \quad (5)$$

$$G(f) = \mathrm{Re}(\gamma/Z) \quad (6)$$

$$C(f) = \mathrm{Im}(\gamma/Z)/2\pi f \quad (7)$$

Figure. 3 show the extracted series resistance R for interconnects with various structure dimensions at room temperature. For fixed spacing between signal line and grounding line, larger signal line width would lead to smaller R. In addition, R increased as frequency increases due to skin effect. At fixed signal line width, the proximity effect causes smaller spacing a larger and more abrupt R than larger spacing. Moreover, process variation causes differences of R at low frequency for fixed signal line width, i.e., different line width bias (the difference between real and drawn signal line width) for different pattern density.

For the extracted series inductance L as shown in Fig. 4, L was composed of two parts: one is frequency independent external component, which is approximately proportional to spacing and inversely proportional to signal line width; another is frequency dependent internal component, which is proportional to skin depth. At low frequency or even DC, external component dominates; hence larger L value is observed for smaller signal line width and larger spacing. As frequency increases, internal component dominates, so that L value decreases because of smaller skin depth. For smaller spacing, smaller skin depth results in more rapid decrease of L by additional proximity effect.

The extracted shunt conductance G, as shown in Fig. 5, increased for larger signal line width and spacing due to more induced loss in substrate. Following the increasing of frequency, G increases in linearly proportional to frequency, hence substrate loss could not be neglected at high frequency.

For larger signal line width and smaller spacing, larger shunt capacitance C was observed as shown in Fig. 6 due to larger area capacitance and coupling capacitance, respectively. In addition, C was a weak function of frequency and decreased slightly as frequency increased.

On the other hand, ambient temperatures would also affect interconnect performances. Fig. 7 shows extracted R for interconnect composed of 2 um in signal line width and 2 um in spacing at high temperature (HT, 125℃), room temperature (RT, 25℃) and low temperature (LT, -25℃), respectively. As ambient temperature increases, R increases for positive temperature coefficient.

Finally, Figs. 8, 9 and 10 present extracted L, G and C under various ambient temperatures, no significant discrepancies are found as temperature changes.

4. Conclusions

In this paper, we present a systematic analysis of interconnects' characteristics for RF applications. With traditional Telegrapher's RLGC model, the effects of layout dimensions and ambient temperatures on the extracted frequency dependent parameters have been investigated in detail. The results are important for modeling interconnects in advanced high frequency circuits in which the spacing is smaller.

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[5]. J. Aguilera, *et. al*, "Design and test of integrated inductors for RF applications, " Kluwer Academic Publishers, Boston, 2003.

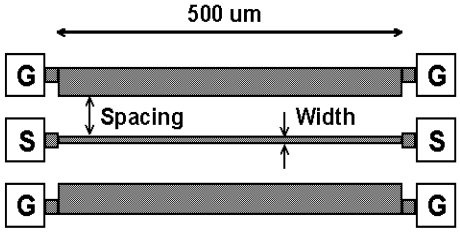

Fig.1 (a) Layout of interconnects in this work with fixed length of 500 um. Variable signal line width and spacing between signal line and grounding line were laid to observe the layout dimension effects on RF performances.

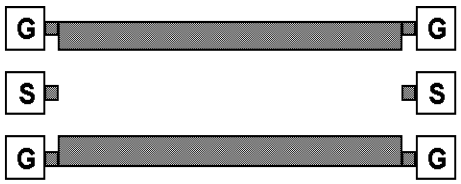

Fig.1 (b) Open dummy structures that removed the signal line of the respective interconnects.

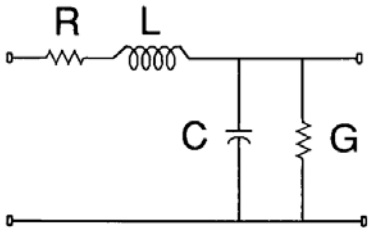

Fig.2 Conventional Telegrapher's RLGC model of unit cell in infinity subsections of interconnects.

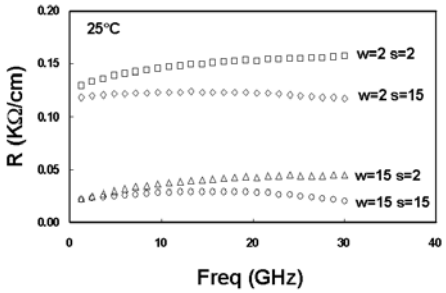

Fig.3 Extracted series resistance R for different layout dimensions of interconnects at room temperature 25°C.

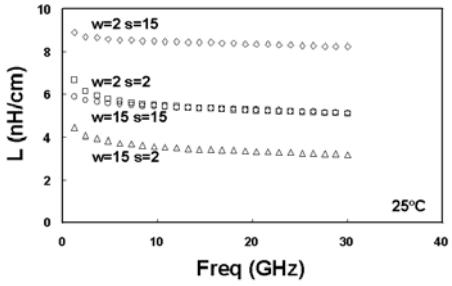

Fig.4 Extracted series inductance L for different layout dimensions of interconnects at room temperature 25°C.

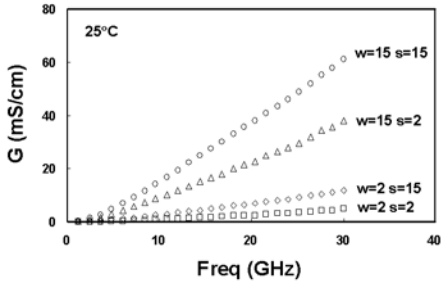

Fig.5 Extracted shunt conductance G for different layout dimensions of interconnects at room temperature 25°C.

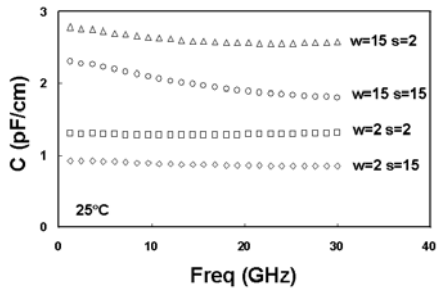

Fig.6 Extracted shunt capacitance C for different layout dimensions of interconnects at room temperature 25°C.

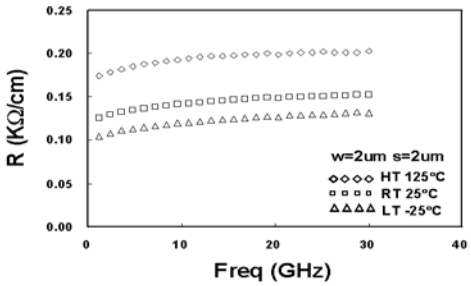

Fig.7 Extracted series resistance R for different ambient temperatures with fixed signal line width of 2 um and spacing of 2 um.

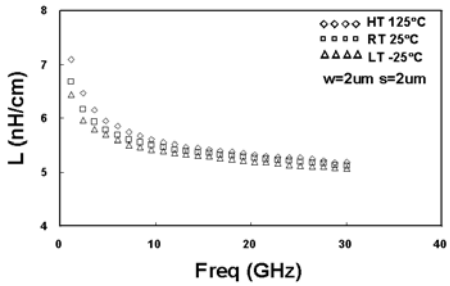

Fig.8 Extracted series inductance L for different ambient temperatures with fixed signal line width of 2 um and spacing of 2 um.

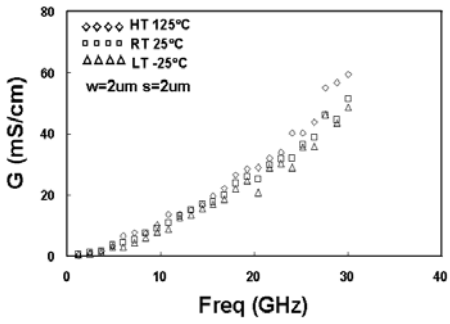

Fig.9 Extracted shunt conductance G for different ambient temperatures with fixed signal line width of 2 um and spacing of 2 um.

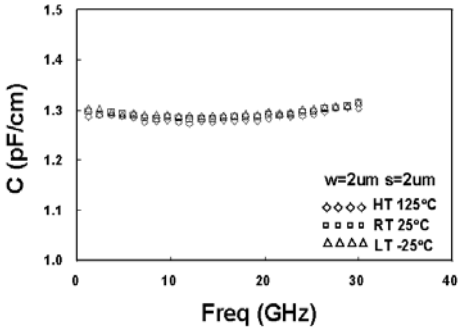

Fig.10 Extracted shunt capacitance C for different ambient temperatures with fixed signal line width of 2 um and spacing of 2 um.