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P-3-1

# An Efficient Mobility Enhancement Engineering on 65nm FUSI CMOSFETs using a Second CESL Process

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## 1. Introduction

As the devices geometry is scaled down continually, some issues such as the boron penetration, poly gate depletion and low carrier mobility become more critical and serious. Metal gate is an efficient approach to eliminate the boron penetration and poly gate depletion [1], and fully silicided (FUSI) is a promising metal gate candidate due to the simplified processing as well as the tunable work function [2]. On the other hand, the high stress contact etch stop layer (CESL) has been used extensively to promote channel carrier mobility in conventional devices [3]. However, very few studies inspected the impact of high tensile stress CESL (TS CESL) on FUSI devices performance yet. In this work, we investigated the device driving capacity, leakages, low frequency noise (LF noise) and C-V characteristics for 65nm Ni-FUSI CMOSFETs with and without the TS CESL.

## 2. Experiments

Devices were fabricated using a modified standard CMOS process. After S/D Cobalt salicidation, the first TS CESL (700A) was deposited (Fig. 1(a): control device). After the inter layer dielectric oxide was deposited, FUSI CMP planarization was adopted to remove the 1st TS CESL down to polysilicon gate. In this work, Ni-silicide has been used for the FUSI technology because of lower thermal budget and better properties [4]. Finally, the Ni-FUSI gate electrode was formed after RTP (Fig. 1(b)). In order to inspect the impact of high tensile stress in Ni-FUSI devices, some Ni-FUSI devices were deposited by TS CESL (700A) (Fig. 1(c)).

## 3. Results

Figure 2 shows the $I_D$-$V_D$ curves for nMOSFETs with $|V_G-V_T|$=1V, it is found that devices with Ni-FUSI gate possess higher driving capacity than control devices do, which is due presumably to the better gate control under the same $V_G$-$V_T$; therefore, larger channel charges will be induced in channel region, lowering the channel resistance. Besides for these Ni-FUSI devices, the driving capacity can be also enhanced by a TS CESL. It implied that the TS CESL is an efficient method to improve driving capacity in Ni-FUSI devices. Fig. 3 shows that Ni-FUSI devices with TS CESL possess the highest $G_{m\,MAX}$. In Fig. 4, because of the positive shift of flatband voltage, the Ni-FUSI devices possess higher threshold voltage ($V_T$) and better subthreshold swing especially for devices with TS CESL. In comparison with control device, the best noise performance was found in Ni-FUSI devices without TS CESL, as shown in Fig. 5. In Fig. 6, the Ni-FUSI devices without TS CESL possess lower junction leakages than the control devices does. For devices with Ni-FUSI gate, lower junction leakages was found, which is due presumably to the smoother band bending in $Si/SiO_2$ interface happen, lowering the accumulated electrons in channel region. On the other hand, we believed that the RTP in FUSI process can also improve the integrity of S/D junctions. And the junction leakage in device with TS CESL is slightly high because of the tensile stress induced defect happen. The gate leakage is shown in Fig. 7, it found that there is no apparent difference between control devices and Ni-FUSI devices; it implied that the process of FUSI CMP didn't induce additional damages to gate oxide. From Fig. 6 and 7, we believed that the LF noise characteristic was mainly affected by junction leakage. In comparison with control device, lower poly gate depletion can be found on Ni-FUSI devices, as shown in Fig. 8. And larger accumulation capacitance is found on Ni-FUSI device without TS CESL because without TS CESL-induced defects happened. For pMOSFETs, the $I_D$-$V_D$ curves were shown in Fig. 9. Similar to the nMOSFETs, those Ni-FUSI devices without TS CESL possess better driving capacity than the control devices does. But for Ni-FUSI device with TS CESL, lower driving current was found because the inappropriate TS CESL-induced tensile stress (should be compress not tensile) will degrade pMOSFET performance. Investigation from the characteristics of $G_m$ (Fig. 10) and $I_D$-$V_G$ (Fig. 11), we found that the TS CESL also caused worse $G_m$ and the subthreshold characteristics ($I_{OFF}$, SS). Similar tendency of LF noise was found on pMOSFETs, as shown in Fig. 12. Compared to control device, the best one was happened on Ni-FUSI devices without TS CESL. We believed that the worst LF noise in control device is affected by larger junction leakages (Fig. 13), not by the gate leakages (Fig. 14). A C-V curve for pMOSFETs was shown in Fig. 15. Similar as nMOSFETs, Ni-FUSI pMOSFETs without TS CESL possess the larger accumulation capacitance.

## 4. Summary

In this work, the driving capacity, leakages, low frequency noise (LF noise) and C-V characteristics were investigated for 65nm FUSI n- and pMOSFETs with and without the TS CESL to inspect the impacts of TS CESL on FUSI devices performance. In nMOSFETs, a TS CESL will improve the driving capacity, but it also induced more defects and enlarged junction leakages, resulting in higher LF noise and decreasing the accumulation capacitance. In pMOSFETs, the TS CESL is profitless for device performance due to an inappropriate stress (should be compress not tensile). Furthermore, we also found that the FUSI process didn't caused apparent damages to the gate oxide for both Ni-FUSI n- and pMOSFETs.

## Acknowledgement

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**References**

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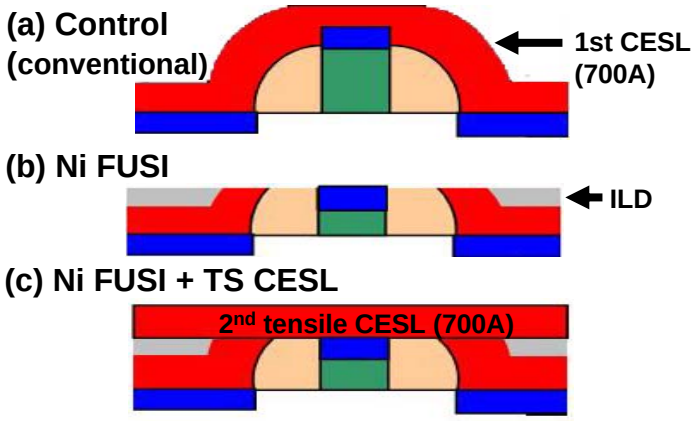


Fig. 1. schematic views of 65nm MOSFETs with various gate electrode (a) conventional gate with 1st CESL (control device). (b) Ni-FUSI gate. (c) Ni-FUSI gate covered with 2nd TS CESL.

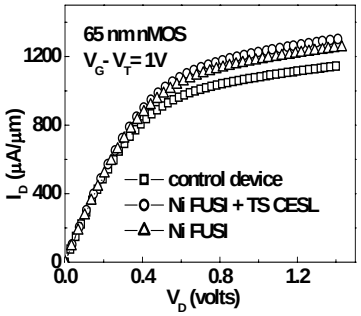


Fig. 2. $I_D$-$V_D$ of 65nm nMOSFETs with various gate electrode. (under $V_G$-$V_T$=1V)

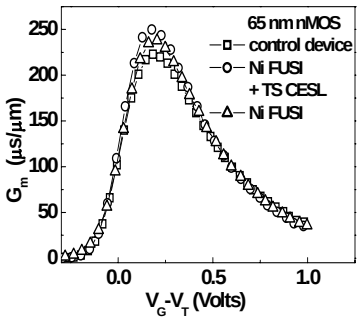


Fig. 3. $G_m$ curves of 65nm nMOSFETs with various gate electrode.

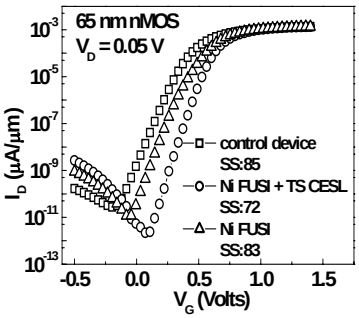


Fig. 4. $I_D$-$V_G$ of 65nm nMOSFETs with various gate electrode.

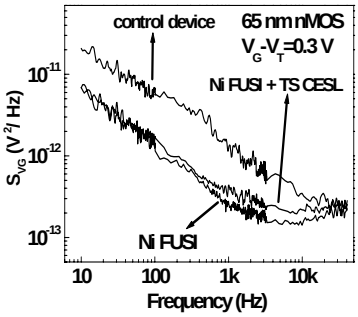


Fig. 5. low frequency noise of 65nm nMOSFETs with various gate electrode. ( freq=10~40kHz, $V_D$= 0.05V)

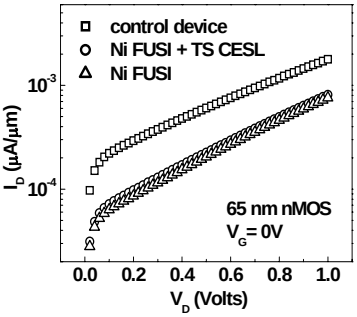


Fig. 6. junction leakages of 65nm nMOSFETs with various gate electrode. ($V_G$= 0V, $V_D$= 0~1V)

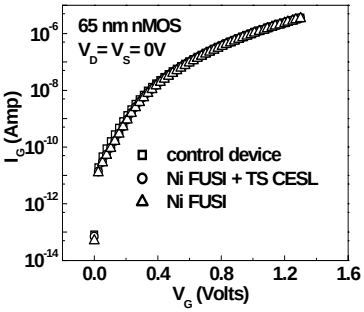


Fig. 7. gate leakages of 65nm nMOSFETs with various gate electrode. ($V_D$=$V_S$= 0V, $V_G$= 0~1.2V)

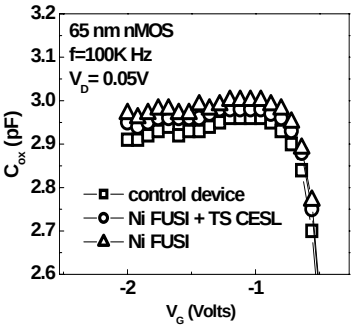


Fig. 8. C-V curves in accumulation region for 65nm nMOSFETs with various gate electrode. ( freq = 100kHz)

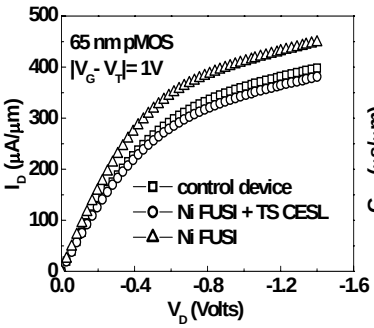


Fig. 9. $I_D$-$V_D$ of 65nm pMOSFETs with various gate electrode. (under $|V_G$-$V_T|$= 1V)

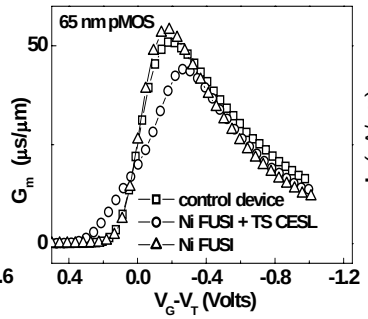


Fig. 10. $G_m$ curves of 65nm pMOSFETs with various gate electrode.

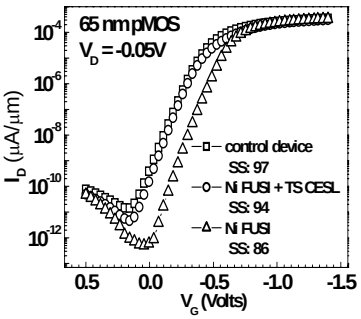


Fig. 11. $I_D$-$V_G$ of 65nm pMOSFETs with various gate electrode.

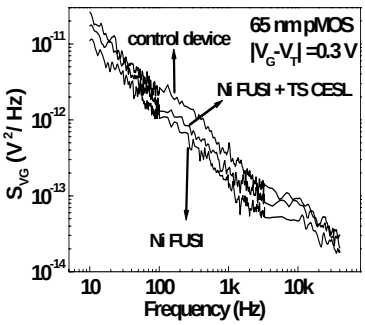


Fig. 12. low frequency noise of 65nm pMOSFETs with various gate electrode. ( freq=10~40kHz, $V_D$= -0.05V)

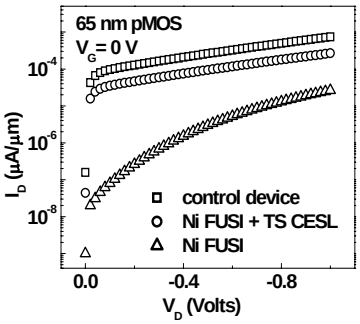


Fig. 13. junction leakages of 65nm pMOSFETs with various gate electrode. ($V_G$= 0V, $V_D$= 0~-1V)

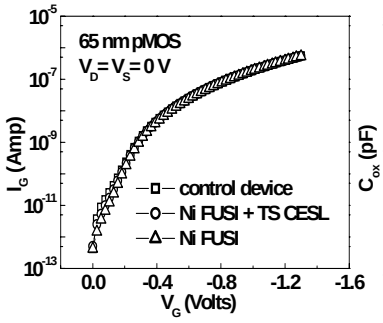


Fig. 14. gate leakages of 65nm pMOSFETs with various gate electrode. ($V_D$=$V_S$= 0V, $V_G$= 0~-1.2V)

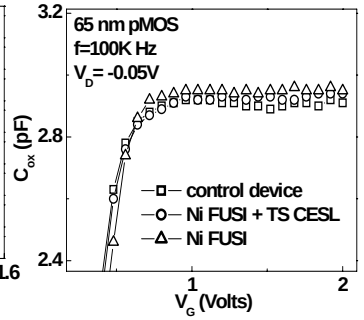


Fig. 15. C-V curves in accumulation region for 65nm pMOSFETs with various gate electrode. ( freq = 100kHz)