P-3-10

Effect of Mobility Degradation and Supply Voltage on NBTI Induced Drain Current Degradation

Jone F. Chen¹, Dao-Hong Yang¹, Chih-Yung Lin², and Shien-Yang Wu²

¹Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan Phone: +886-6-2757575 E-mail: jfchen@mail.ncku.edu.tw

²Logic Technology Division/R&D, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan

1. Introduction

Negative Bias Temperature Instability (NBTI) in pMOSFETs is a major reliability concern to continued device scaling. The degradation behavior, mechanism, degradation model, and recovery behavior have attracted widely attention recently [1]-[7]. However, there is little report to address the correlation between drift in device electrical parameters.

In this work, NBTI of state-of-the-art pMOSFETs fabricated with dual gate oxide thickness (Tox) is investigated. Results indicate that mobility degradation is significant in the device with thinner Tox. Further, the effect of mobility degradation on Id degradation was analyzed. Finally, a model is established to evaluate the impact of supply voltage (Vdd) on Idsat degradation.

2. Experiments

pMOSFETs used in this work were fabricated by an advanced dual gate CMOS process with dual gate oxide thickness. Tox (EOT) is 1.4nm, 5.6nm for the core and I/O device, respectively. To investigate the NBTI induced degradation, dc stress with various Vg was applied to the gate under various temperatures with the source, drain, and substrate tied to the ground. Idsat and Idlin were monitored under Vg=Vdd, Vd=Vdd or -50mV. V_T was extracted under Vd=-50mV. The temperature of stress and measurement is identical during each experiment.

3. Results and Discussion

Fig. 1 shows the typical result of Id degradation and V_T shift for the device stressed under similar Eox. Krishnan et al. has reported that Id degradation resulted from ΔV_{T} can be expressed as follows [2]:

$$\Delta \operatorname{Idlin} / \operatorname{Idlin} \approx -\Delta V_{T} / (Vg - V_{T})$$
(1)

$$\Delta \operatorname{Idsat} / \operatorname{Idsat} \approx -\theta \Delta V_{T} / (Vg - V_{T})$$
(2)

where $1 < \theta < 2$. Note that mobility degradation is ignored in deriving Eqs. 1 and 2. To verify the validity of Eqs. 1 and 2, Figs. 2 and 3 analyze Idlin and Idsat degradation as a function of $-\Delta V_T/(Vg-V_T)$. As seen in Fig. 2, data of Tox=5.6nm device stressed under various Eox and temperatures exhibit a slope of 1.02, very close to 1 as in Eq. 1. However, Idlin degradation data of Tox=1.4nm device has a slope of 1.64, indicating mobility degradation is not negligible in Tox=1.4nm device.

This argument can be confirmed from Fig. 4, where split C-V measurement was performed to measure the mobility. Fig. 4 shows the fresh and aged mobility data for devices stressed to reach the same $\Delta V_T/(Vg-V_T)$. According to Eq. 1, devices should exhibit similar Idlin degradation if mobility degradation is truly negligible. However, Figs. 4 and 5 reveal that Tox=1.4nm device has large mobility degradation. To explain enhanced mobility degradation in Tox=1.4nm device, ΔV_T is expressed as:

$$\Delta V_{\rm T} = -\left(\Delta Qit + \Delta Qot\right) / \operatorname{Cox} \tag{3}$$

where ΔQit is interface state generation, while ΔQot is positive charge trapping. Since mobility degradation has a strong correlation with ΔQit [8], our data suggest that ΔV_T in Tox=1.4nm device is mainly resulted from ΔQit . On the other hand, ΔV_T in Tox=5.6nm device is mainly resulted from ΔQot in the gate oxide.

According to data in Figs. 2 and 3, the new model to correlate ΔV_T and Id degradation can be established as follows:

> Δ Idlin / Idlin $\approx -m_1 \Delta V_T / (Vg - V_T)$ (4)

 Δ Idsat / Idsat $\approx -m_2 \Delta V_T / (Vg - V_T)$ (5)where m_1 is the slope in Fig. 2 that can be used to represent the severity of mobility degradation. m_2 is the slope in Fig. 3 and its value is affected by both mobility degradation and carrier velocity saturation.

Because the same device may operate under various Vdd, the effect of Vdd on Idsat degradation is necessary to explore. The relationship between $(Vg-V_T)$ and Idsat measured under Vg=Vd=Vdd is analyzed in Fig. 6. Data indicate that Idsat \propto (Vg-V_T)^m, where m is 1.53 and 1.83, very close to m_2 extracted from Fig. 3. Such a result suggests that Eq. 5 can be used to model Idsat degradation under various Vdd since $\Delta Idsat/Idsat \approx - m\Delta V_T/(Vg-V_T)$ if Idsat $\propto (Vg-V_T)^m$ is valid. To verify the above argument, Fig. 7 shows the Idsat degradation as a function of Vdd for the Tox=5.6nm device stressed under various time. The model calculated by Eq. 5 using m₂ extracted from Fig. 3 matches with data pretty well. Fig. 8 shows the Idsat degradation as a function of Vdd for both Tox=5.6nm and 1.4nm devices. Reasonably good fitting between data and model indicates that Eq. 5 and the results in Fig. 3 can be used to predict the impact of Vdd on Idsat degradation.

4. Conclusions

NBTI in advanced pMOSFETs with dual gate oxide thickness was investigated. The correlation between Id degradation and V_T shift was discussed. Further, a model to predict Idsat degradation under various Vdd has been established. Such an investigation can lead to a thorough understanding on the NBTI of advanced MOS devices.

Acknowledgements

This work was partially supported by National Science Council under contract NSC94-2215- E006-061.

References

- [1] N. Kimizuka et al., VLSI Tech. Sym. Dig. (2000) 92.
- [2] A. T. Krishnan et al., Tech. Dig. IEDM (2003) 349.
- [3] D. K. Schroder et al., J. Appl. Phys., 94 (2003) 1.
 [4] V. Reddy et al., Proc. IRPS (2002) 248.
 [5] S. Chakravarthi et al., Proc. IRPS (2004) 273.

- [6] H. Aono et al., Proc. IRPS (2004) 23. [7] S. Rangan et al., Tech Dig. IEDM (2003) 341.
- [8] M Denais et al., IEEE Trans. Dev. and Mat. Reli., 4 (2004) 715.



Fig. 1 The typical result of Id degradation and $V_{\rm T}$ shift for the device stressed under similar Eox.



Fig. 2 Δ Idlin / Idlin $\approx -m_1 \Delta V_T$ / (Vg - V_T). m_1 can be used to represent the severity of mobility degradation.



Fig. 3 Δ Idsat / Idsat $\approx -m_2 \Delta V_T$ / (Vg - V_T). m_2 is affected by both mobility degradation and carrier velocity saturation.



Fig. 4 Fresh and aged mobility for devices stressed to reach the same $\Delta V_T/$ (Vg - $V_T).$



Fig. 5 Tox=1.4nm device exhibits much larger mobility degradation.



Fig. 6 Idsat measured under various Vdd indicates that Idsat \propto $(Vg-V_T)^m$, where m is very close to m₂ extracted from Fig. 3.



Fig. 7 Idsat degradation as a function of Vdd. Model matches with data pretty well under various stress time.



Fig. 8 Idsat degradation as a function of Vdd. Model fits data pretty well in both Tox = 5.6nm and 1.4nm device.