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Impact of Source/Drain $Si_{1-y}C_y$ Stressors on the Silicon-on-Insulator NMOSFETs

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1. Introduction

Strain engineering in the channel region of metal-oxide-semiconductor field-effect (MOS) transistors is being actively pursued to enhance the drive current. A stressor in the vicinity of the channel is usually employed for channel strain engineering. A relaxed silicon-germanium (SiGe) layer underlying a Si channel region may be used as a bottom stressor in order to introduce biaxial strain for the improvement of carrier mobility [1-2]. A top stressor such as a high stress silicon nitride film formed over a transistor structure, was also employed to enhance the electron mobility [3-4]. Recently, Silicon-on Insulator (SOI) [5] NMOSFETs with silicon-carbon (SiC) alloy source/drain (S/D) regions have been demonstrated [6-7], while relatively little is know about the stress effects in devices such as the magnitude and distribution of stress components, the origin of the stress field, and their relationship to electron mobility enhancement. In the present paper, we perform a theoretical evaluation of the stress field in the SOI NMOSFET with lateral lattice-mismatched SiC source/drain (S/D) stressors. The dependence of the stress components on transistor design parameters such as inter-stressor spacing, stressor lattice constant, stressor recessed depth, stressor raised height, and alloy mole fraction in stressors is investigated. The electron mobility enhancement and potential scalability of the transistor structure are also discussed.

2. Device Structure

Figure 1 shows the SOI NMOSFET with $Si_{1-y}C_y$ stressors in the source and drain regions. The spacing L_G between the stressors, the C mole fraction y, h and d are varied. The theoretical limit to the amount of channel stress is determined by the maximum stress that can be generated at the Si/SiC interface before dislocation are generated; this depends directly on the carbon mole fraction. This limit is defined by the following equation $\sigma=E*\varepsilon/(1-v)=76.5*y$ (GPa) where E is silicon Young's modulus, v is silicon Poisson's ratio, and ε is the strain induced by the difference of the Si and $Si_{1-y}C_y$ lattice constants (ε=0.34*y). For a given carbon mole fraction the amount of stress in the channel is determined by etch depth, which correlates to the SiC thickness, and the etch shape. In this paper, the recess etch shape is anisotropic. The commercial process simulator FLOOPS-ISE™ [8] was performed to study the stress field in the transistor structure. The $Si_{1-y}C_y$ stressors affect two major strain components, the lateral stress σ_{xx} and the vertical stress σ_{yy}. If the lattice of $Si_{0.99}C_{0.01}$ is fully strained to assume the lattice constant of the underlying Si substrate, then the value of strain in the $Si_{0.99}C_{0.01}$ source/drain region will be 0.5%, and there will be no strain in the Si substrate. The partially relaxed SiC stressors in the source and drain regions tense the Si channel laterally, leading to a large tensile stress σ_{xx} that extends throughout the channel region.

3. Results and Discussions

Figures 2-5 show the impact of inter-stressor spacing L_G, the recess depth d, raised height h, and C content y in the $Si_{1-y}C_y$ stressors on the spatially stress components in the channel region, respectively. Increasing the stressor height h in a raised S/D structure while maintaining the same stressor depth d leads to a more tensile stress σ_{xx} (Fig. 2). Figure 3 shows that for a given L_G, of 50 nm and C content of 1 %, increasing the depth of the SiC stressor, increases lateral stress σ_{xx} in the Si channel while slightly decreases vertical stress σ_{yy} in that one. For a given L_G, of 50 nm and d=60 nm, increasing the C mole fraction y, i.e., the lattice mismatch between the SiC stressor and the channel, increases the magnitude of both σ_{xx} and σ_{yy} linearly (Fig. 4). For a given y of 1% and d=60nm, decreasing L increases the magnitudes of both σ_{xx} and σ_{yy}, as shown in Fig. 5. In general, σ_{xx} is more uniformly distributed and is larger in magnitude than σ_{yy}. The electrical characteristics of the SOI NMOSFETs were simulated with DESSIS™ [8] using the strain-induced mobility models [9-10] to account for the change of mobility in highly strained regions. We perform a spatial averaging of the stress components over the region where the inversion electron resides, and use the spatially averages stress components to get the mobility enhancement. The mobility enhancement is approximately the same as drain current enhancement in linear region as used in Ref. [11]. In generally, the contribution of lateral stress σ_{xx} to mobility enhancement is larger than that of vertical stress σ_{yy}. The ITRS [12] target 100% mobility enhancement in the year 2007 is easily achievable with L_G, =50nm, d=60 nm h=20 nm, and y=1% as shown in Fig. 6. The thick lines are drawn with L_G, of 5nm, 50nm, 100nm, and 180nm to guide the eye for the purpose of the optimal design. The thin lines are drawn with increasing d to guide the eye for the similar purpose. Fig. 7 plots the threshold voltage shift for the carbon mole fraction with 4 sets of L_G and a fixed d of 60 nm and h of 20 nm. Also included are the data for the different values of d (10 nm, 20 nm, 40 nm, 60 nm, 80nm, and 100 nm) at the carbon content of 1 % and L_G of 50 nm. All the threshold voltage shifts are lower than the value of 50 mV. This means that the stress in such a transistor induces a relatively lower band gap reduction and that the variation of the threshold voltage shift is not serious.

4. Conclusions

In conclusion, the stress field in a SOI NMOSFET with the SiC source/drain stressors was investigated and the origin of the strain field in the transistor channel was clarified. Reducing the inter-stressor spacing and increasing the C content and the recessed depth/ raised height of the SiC stressors are three ways to achieve high strain levels in the Si channel region for drive current and enhanced electron mobility in n-channel metal–oxide–semiconductor transistors.

References

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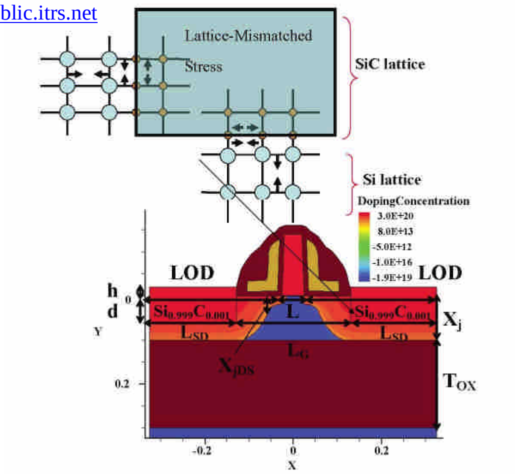

Fig. 1 Schematic of Silicon-on-Insulator NMOSFET with $Si_{1-y}C_y$ stressors in source and drain regions. The inset illustrates the crystal lattices in the vicinity of the vertical and horizontal heterojunctions, with arrows indicating the nature of the stresses experienced by the crystal lattices. Oxide box thickness Tox is 200 nm. The arrows indicate the nature of the stresses experienced by the crystal lattices. Xj is the deep source/drain junction depth and X_{jDS} is the source/drain extended junction depth. Note that L is channel length and L_G is stressor spacing.

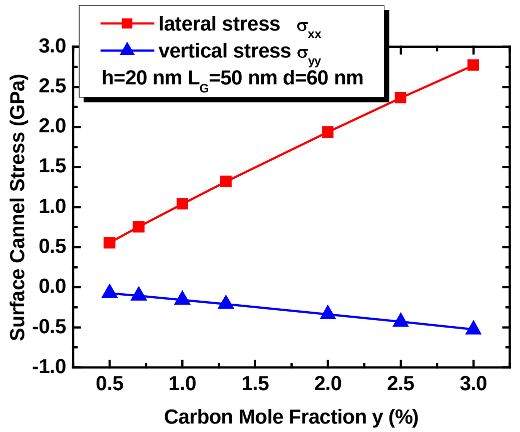

Fig. 4 Lateral and vertical strain components, σ_{xx} and σ_{yy}, respectively, in the surface channel plotted as a function of the C mole fraction *y* in the $Si_{1-y}C_y$ stressor.

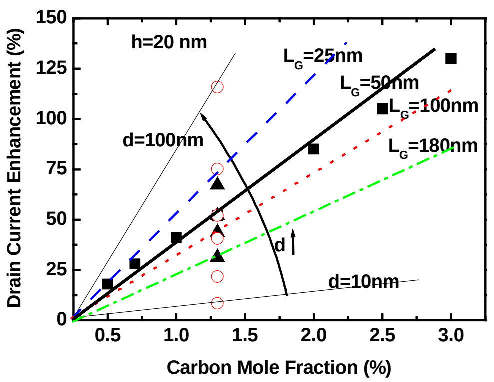

Fig. 6 Increasing the Carbon mole fraction in $Si_{1-y}C_y$ stressor and reducing L_G and larger d leads to larger lateral stress σ_{xx} and vertical stress σ_{yy}. The solid squares denote the case of L_G=50nm and d=60nm. The solid triangles denote the case of L_G=50nm and carbon mole fraction of 1%. The open circles denote the case of L_G=50nm and carbon mole fraction of 1%. Where h=20nm is used in all cases.

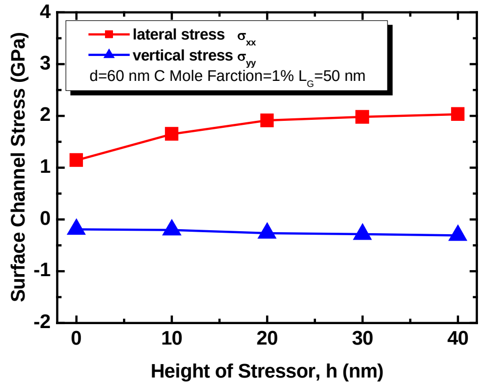

Fig. 2 Raising the stressor height h leads to more tensile lateral stress σ_{xx}.

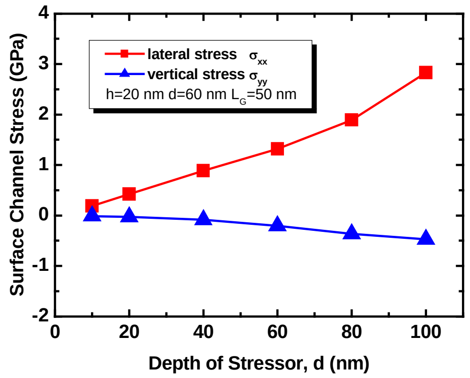

Fig. 3 Lateral and vertical strain components, σ_{xx} and σ_{yy} , respectively, in the surface channel plotted as a function of the depth of the $Si_{1-y}C_y$ stressor.

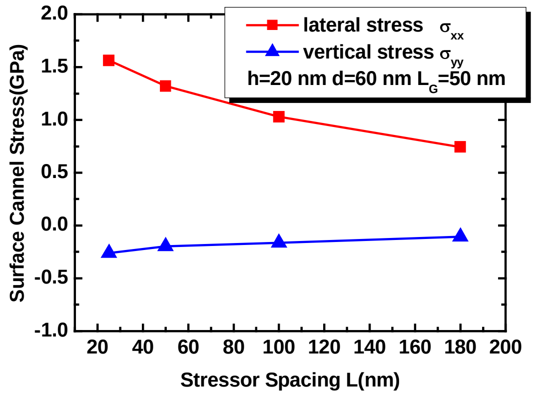

Fig. 5 Lateral and vertical strain components, σ_{xx} and σ_{yy}, respectively, in the surface channel plotted as a function of the spacing between the source stressor and drain stressor.

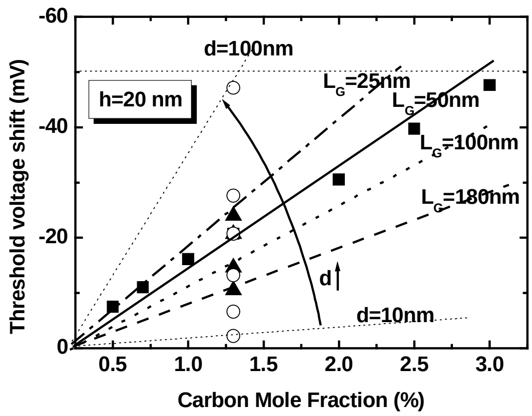

Fig. 7 Increasing the carbon mole fraction in $Si_{1-y}C_y$ stressor and reducing the inter-stressor spacing and the larger stressor depth lead to larger magnitudes of the lateral stress (σ_{xx}) and the vertical stress (σ_{yy}). The threshold voltage shift results to the strain-induced band gap reduction. The maximum threshold voltage shift of 50mV is observed. The solid squares denote the case of L_G=50nm and d=60nm. The solid triangles denote the case of d=60nm and carbon mole fraction of 1%. The open circles denote the case of L_G=50nm and a carbon mole fraction of 1%.