Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 524-525

P-3-13

Modeling of Drain Bias Dependence on Threshold Voltage Shift Under Negative Gate Bias Stress of a-Si:H TFTs

Huai-Yuan Tseng, Ko-Yu Chiang and Chen-Pang Kung

Flexible Electronics Technology Division / Electronics and Optoelectronics Research Laboratories (EOL)

Industrial Technology Research Institute (ITRI)

Bldg. 51, No. 195, Sec. 4, Chung Hsing Rd., Chutung, Hsinchu, Taiwan, R.O.C.

Phone: +886-3-591-7669 Fax: +886-3-582-0052 E-mail: HYTseng@itri.org.tw

1. Introduction

Hydrogenated amorphous silicon thin film transistor (a-Si:H TFTs) is one of the significant components for liquid crystal display (LCD) industry. For LCD applications, a-Si:H TFTs were used as pixel switches, where the threshold voltage (V_T) shift will not occur because of the short duty cycle operation [1]. However, when a-Si:H TFTs were adopted as analog driving devices in AMOLED pixels [2] or sensor circuits [3], V_T shift become noticeable under prolong gate and drain bias. Several researches have been done to understand the V_T instability under DC gate bias [4], pulse gate bias [5], however none of them were suitable for analog application since drain voltage was neglected in these works. Karim et al. proposed a drain-bias dependence of V_T stability [6]. Unfortunately, in his work, the drain-bias dependence on negative gate bias stress was not discussed.

In this study, an attempt was made to derive a model of drain-bias dependence on V_T shift of a-Si:H TFTs under negative gate bias stress, which is an important information needed for reverse bias annealing technique [7]. The model derived in this work is also one of the key parts for precise reliability simulation of a-Si:H TFT circuits.

2. Experimental

The a-Si:H TFTs used in this work were traditional inverted staggered type with back channel etch structure. 350nm a-SiNx film was used as gate insulator and 200nm a-Si:H was used as semiconductor layer. The dimension of the devices used for different drain voltage testing were fixed at W/L=80/12. All the stress experiments were measured using Agilent 4156A and threshold voltages were extracted from the transfer curves (I_D-V_G) using the traditional maximum transconductance method. During the stress test, each V_T was extracted by interrupting for 10 sec. All of the measurements were done at room temperature.

3. Results and Discussions

Fig. 1 shows the V_T shift versus stress time. The stress condition was V_{GS} = -15V while V_{DS} varied from 0V to 20V in 5V step. The test results showed that the V_T shifted more negatively when V_{DS} increased. Pure negative V_T shift without turn-around phenomenon [8] implies the charge trapping mechanism [9] dominated the V_T shift.

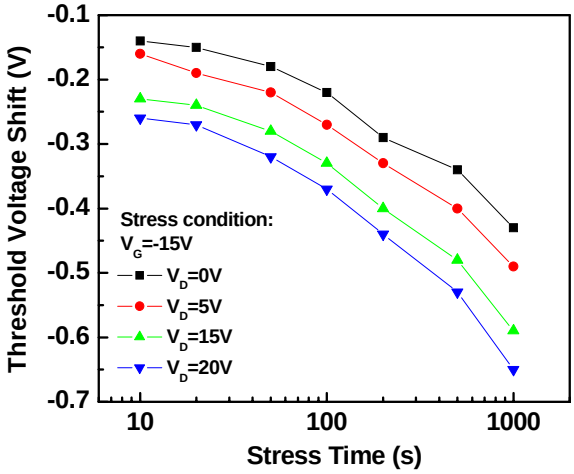

Fig. 1 V_T shift versus stress time under various drain bias

From the results, we derived a V_T shift model base on the charge dependence upon charge trapping assumption. Considering the drain bias dependence upon negative gate bias stress, the V_T shift model is proposed by the conventional stretch-exponential function [10] combining with the correction function $f^{-}(V_D)$ as shown below:

$$\Delta V_T^{-}(t,V_D) = \Delta V_T^{-}(t) \cdot f^{-}(V_D) \quad (1)$$

$$\Delta V_T^{-}(t) = -(V_T - V_G)^{\alpha}\left\{1-\exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \quad (2)$$

where α, β, τ are fitting parameters.

When negative V_{GS} and positive V_{DS} were applied to the device simultaneously, the potential distribution along

the channel region of a-Si:H TFT can be depicted as Fig. 2.

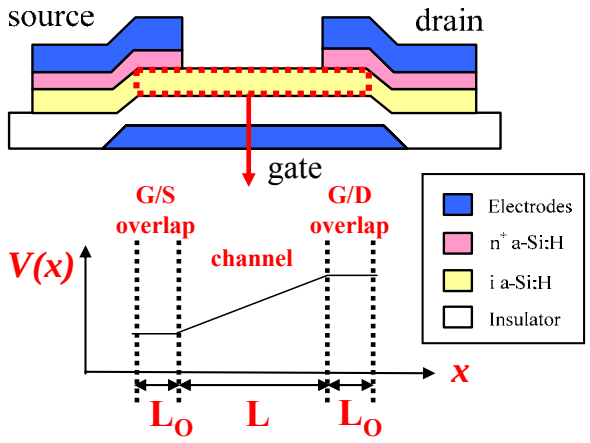

Fig. 2 Potential distribution along channel of the a-Si:H TFT

Based on the gradual channel approximation, the potential along the channel region is a linear function. Therefore, the concentration of induced hole within a unit length can be expressed as

$$n_{h^+}(x,V_D) = W \cdot \frac{C_{SiNx}}{q} \cdot \left[V_T - V_G + \frac{V_D}{L} \cdot x \right] \cdot dx \qquad (3)$$

where C_{SINx} is the gate capacitance per unit area, W is the channel width, and L is the channel length. The total hole concentration under negative V_{GS} and positive V_{DS} can be obtained by integrating the hole concentration from x=0 to x=L+2L_O based on equation (4), where Lo denotes the length of gate to source/drain overlap. The correction function $f^-(V_D)$ can then be obtained by equation (4) divided by equation (5) which is the hole concentration under zero drain bias.

$$n_{h^+-total}(V_D) = \int_0^{L+2\cdot L_O} n_{h^+}(x,V_D) \cdot dx \qquad (4)$$

$$n_{h^+-total}(0) = \int_0^{L+2\cdot L_O} W \cdot \frac{C_{SiNx}}{q} \cdot [V_T - V_G] \cdot dx \qquad (5)$$

$$f^-(V_D) = \frac{n_{h^+-total}(V_D)}{n_{h^+-total}(0)} = 1 + \frac{L^2 + 2 \cdot L_O}{2L \cdot (L + 2 \cdot L_O)(V_T - V_G)} \cdot V_D \qquad (6)$$

Fig. 3 shows the precise fitting result based on the V_T shift model equation (1) as proposed in this work. The fitting parameters of equation (1) are listed in Table I.

4. Conclusions

An equation for V_T shift under negative gate and positive drain biases was derived based on the charge dependence model, which can be further applied to the complete V_T shift model of a-Si:H TFTs with pulse gate and pulse drain bias stress in future development. A reliability simulator for a-Si:H TFT circuits comprising V_T shift modules can be accomplished when the modeling work is completed. With the precise simulation platform, robust a-Si:H TFT circuits for various applications will be demonstrated in the near future.

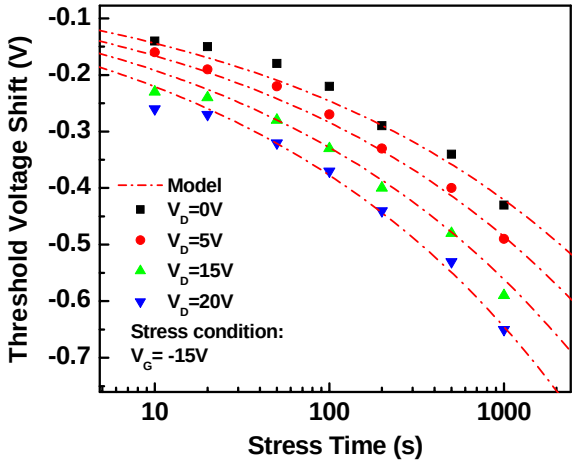

Fig. 3 Fitting results of model Eq. (1) to the experiment data

Table I Fitting parameters of Eq. (1) in Fig. 3

V_G	-15V	L	12 μm	L_O	4 μm
α	1.45	β	0.23	τ	1.57×10^{12}
V_D	$f^-(V_D)$		V_T-V_G		
0	1		16.8		
5	1.091		17.45		
15	1.275		17.3		
20	1.350		18.1		

Acknowledgments

We would like to express sincere thanks to Display Technology Center of ITRI and for providing the measurement samples and the Nanoelectronics Division of EOL/ITRI for their measurement equipment support.

References

[1] C. S. Chiang, J. Kanicki, Jpn. J. Appl. Phys. **37** (1998) 4704

[2] J. H. Jung, H. Kim, et al., SID (2005) 1538.

[3] K. S. Karim, A. Nathan, J. A. Rowlands: IEDM (2002) 215.

[4] F. R. Libsch, J. Kanicki: Appl. Phys. Lett. **62** (1993) 1286.

[5] R. Oritsuki, T. Horii, et al., Jpn. J. Appl. Phys. **30** (1991) 3719

[6] K. S. Karim, A. Nathan et al.: Elec. Dev. Lett. **25** (2004) 188.

[7] J. H. Lee, C. W. Han, et al., IDW (2004) 541

[8] C. H. Huang, J. W. Tsai, et al., Jpn. J. Appl. Phys. **39** (2000) 5763

[9] M. J. Powell: Trans. on Elec. Dev. **36** (1989) 2753.

[10] F. R. Libsch: IEDM (1992) 681