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A New Statistical Evaluation Method for the Variation of MOSFETs

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1. Introduction

With the scaling-down of MOS LSI device, the variation of electrical characteristics in MOSFETs becomes larger and larger. As the result, the circuit design, especially analog circuit design, and the development of device and process become very difficult. Thus understanding variation of the characteristic of devices in a short time is strongly required. However, we cannot evaluate statistical variation and local variation because the number of MOSFETs to be analyzed is very limited and large area is occupied for each MOSFET in the conventional Test Element Group (TEG). Some statistical evaluation methods have been reported.[1]-[4] However, these take relatively long time for the measurement and are difficult to increase the number of MOSFETs.

We have developed and demonstrate the new TEG which is able to understand the statistical and local characteristic variation of MOSFETs in a very short time.

2. New TEG Concept and Experimental

Figure 1 shows the schematic view of the proposed n-MOSFET array. This test structure is composed of the MOSFET array (A) to measure their characteristics, the horizontal and vertical shift register circuits (B,C) to select one of the measured MOSFETs, the source follower circuit (D) to amplify the output signal and the current source transistors (E). Solid line circle in fig.1 shows the MOSFETs to be measured. In this experiment, we use this TEG which is composed of 128×256 MOSFET array (32,768 MOSFETs) with an interval of 40 μm between unit cells. The gate lengths and widths of MOSFETs are shown in Table1.

The measurement method of the MOSFET characteristic is explained in Fig.2. The constant current (I_{ref}) is defined by applying voltage (V_{ref}) to the current source transistor. When the gate voltage (ϕ x) of the switch transistor is biased to high level signal according to the vertical shift register circuit, the output voltage (V_{out}) is shown as following equation (1).

$$V_{out} = V_G - V_{gs} \quad (1)$$

where V_G is applied gate voltage and V_{gs} is the voltage difference between the gate and source of the measured MOSFET. Therefore, we can obtain the V_{gs} when Iref in the MOSFET flows, and V_{gs}-I_{ds} characteristic by changing I_{ref}.

The important point of this circuit is that the V_g-I_d characteristics in MOSFETs are measured by measuring the voltage signals V_{gs}, not the current signals. Thus, by using this circuit, we can obtain a large number of MOSFETs in a very short time. (32,768 MOSFETs are measured in about 0.1 seconds)

The TEG is fabricated using 0.35μm, 1 poly 1 metal CMOS technology. The TEG measured at V_G=2.2V, V_{REF}=0.9V, V_{DD}=3.3V. When Iref is about 1μA, the V_{gs} corresponds to the threshold voltage.

3. Results

In Fig.3, the measured V_{gs} of 32,768 MOSFETs (4,096 MOSFETs each gate area size) is shown as a gray scale. Each pixel corresponds to each MOSFET. The rougher this picture is, the larger the V_{gs} variation is. Then, we can easily realize that the V_{gs} variation of MOSFETs with L= 0.35 μm, W= 0.5 μm is larger than that of any others. Solid line circles in Fig.3 C7 and G1 show the positions of local MOSFETs with anomalous high and low V_{gs}, respectively.

Figure 4 (a) shows V_{gs} of MOSFETs with L= 0.35 μm, W= 0.5 μm on the whole area of the wafer, and Fig.4 (b) shows the enlargement of D5 in Fig.3. The average of V_{gs} of MOSFETs near the edge of wafer is very lower than that near the center as shown in Fig.4 (a). In Fig.4 (b), the some neighboring MOSFETs are shown as the black and the white. The experimental results show that the difference of Vgs of the neighboring MOSFETs with interval of 40μm is even as high as about 100mV.

Figure 5 shows the standard deviation (σ) of V_{gs} as the function of $(LW)^{-1/2}$. Here, σ (V_{gs}) is shown as following equation (2) in this experiment.

$$\sigma(V_{gs}) = \frac{6.8}{\sqrt{LW}} \quad (\text{mV}) \quad (2)$$

σ is proportional to $(LW)^{-1/2}$. This agrees to some papers which have been reported.[1]-[5] This result shows that σ of V_{th} will increase more than 100 mV at 45 nm technology node. This means that reducing of V_{th} variation is strongly required.

Figure 6 shows the distribution of V_{gs} of 223,936 MOSFETs with L= 0.35 μm, W= 0.5 μm and L= 10 μm, W= 10 μm in a wafer. δ(V_{gs}) in the figure is defined as the difference of V_{gs} value in each MOSFETs from the average of V_{gs}. As shown in the figure, we found no anomalous MOSFETs with L= 10 μm, W= 10 μm, that appear out of the main distribution, while we found 6 anomalous MOSFETs with L= 0.35 μm, W= 0.5 μm. The existence probability of the anomalous MOSFETs is 2.7×10^{-5}.

4. Conclusion

We have proposed the new TEG which enables us to understand the statistical and local characteristic variation of MOSFETs in a very short time. By using this TEG, we obtained the statistical distribution of characteristic variation of 223,936 MOSFETs per one size on a wafer and find the positions of anomalous MOSFETs. These results show that the new TEG is a very important and useful tool to understand the statistical variation for scaled-down devices and analog circuit design, and to develop the process technology to reduce the statistical and local characteristic variation.

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References

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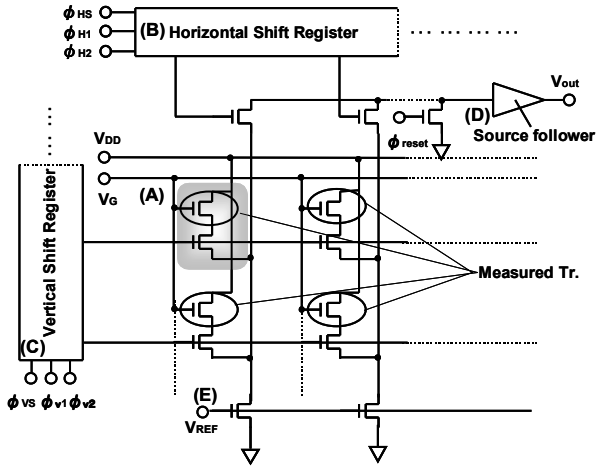

Fig.1 The circuit schematic view of the proposed new evaluation MOSFET array TEG. MOSFETs in solid line circle shows the measured MOSFETs.

Table.1 The gate lengths and widths of MOSFET in the TEG

L[um]	0.35	0.45	0.35	0.45	1	1	3	10
W[um]	0.5	0.7	1.0	1.0	1	3	1	10

4096 (128 × 32) MOSFETs each size

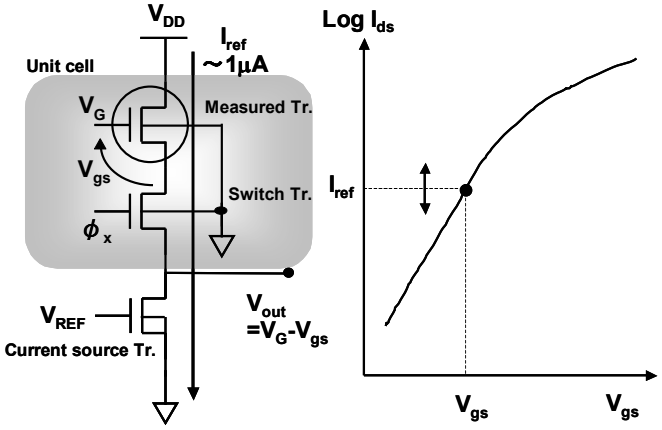

Fig.2 Measurement method of MOSFET characteristics. We can obtain V_{gs} by measuring V_{out} and the characteristic of transistor by changing I_{ref} in a very short time. (A MOSFET is measured in 1.5 μsec.)

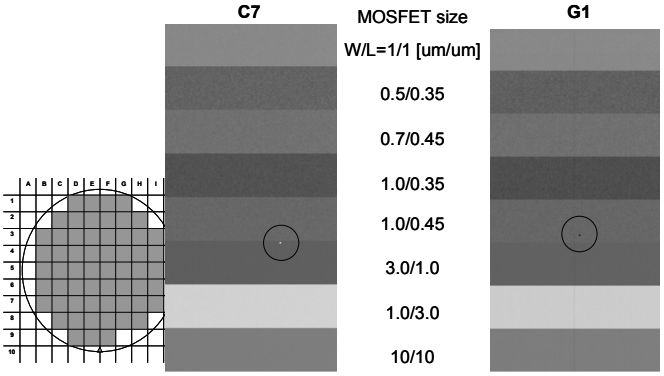

Fig.3 The voltage V_{gs} of the measured MOSFETs is showed as a gray scale. A pixel means the V_{gs} of a MOSFET. A white pixel in solid line circle indicates a local transistor with high V_{gs}. (C7) A black pixel in solid line circle indicates that a local transistor with low V_{gs}. (G1)

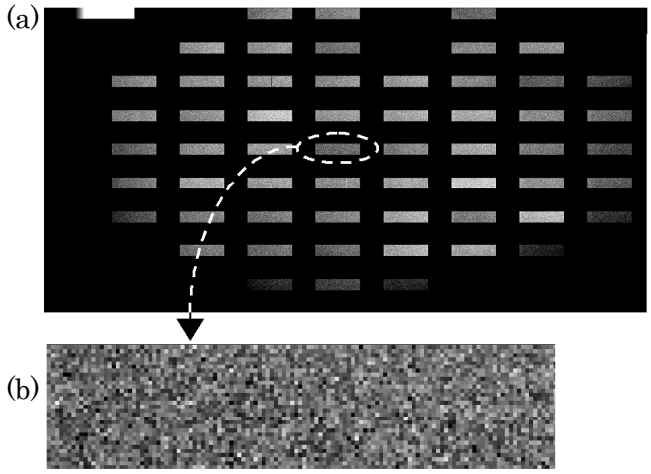

Fig.4 (a) V_{gs} of on the whole area of wafer is showed as a gray scale.(L = 0.35 μm, W = 0.5 μm)
(b)The enlargement of the part of D5 in Fig. 3.
It indicates that the V_{gs} of MOSFETs near the edge of wafer is lower compared with that near the center.

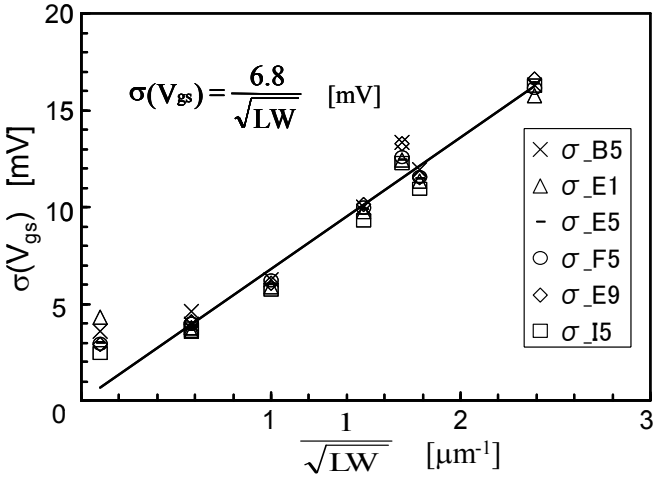

Fig.5 The standard deviation (σ) of V_{gs} as a function of $(LW)^{-1/2}$.

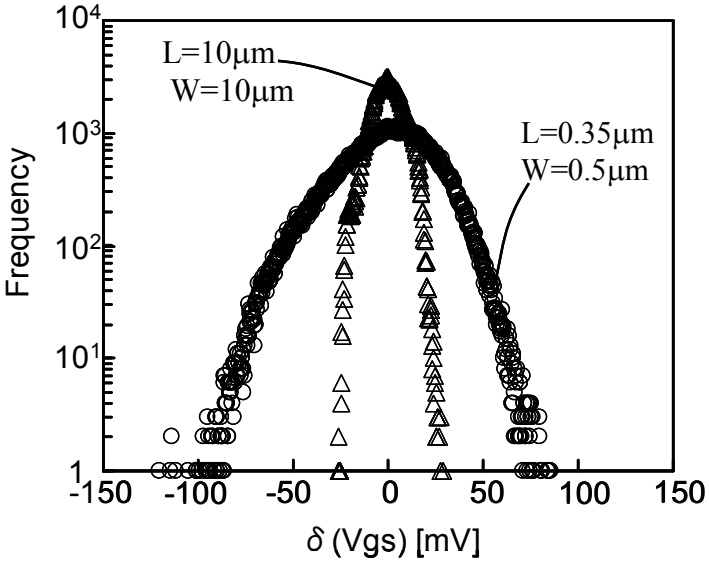

Fig.6 δ (V_{gs}) distribution of 223,936 MOSFETs with L= 0.35 μm, W= 0.5 μm and L= 10 μm, W= 10 μm.
It shows that there are some anomalous MOSFETs with L= 0.35 μm, W= 0.5 μm.