Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 534-535

P-3-18

# A Novel Self Aligned Design Adapted Gate All Around (SADAGAA) MOSFET including two stacked Channels : A High Co-Integration Potential

R.Wacquez[1,2,3], R.Cerutti[1], P.Coronel[1], A.Cros[1], D.Fleury[1], A.Pouydebasque[4], J.Bustos[1], S.Harrison[4], N.Loubet[1], S.Borel[3], D.Lenoble[1], D.Delille[4], F.Leverd[1], F.Judong[1], MP.Samson[1,3], N.Vuillet[1,3], B.Guillaumot[1,3], T.Ernst[3], P.Masson[2], T.Skotnicki[1]

[1)]ST Microelectronics, 850 rue J.Monnet, BP. 16, 38921 Crolles, France . e-mail : thomas.skotnicki@st.com
[2)] L2MP, UMR-CNRS 6137, IMT Technopôle Château Gombert, 13451 Marseille France
[3)]LETI, rue des Martyrs, 38054 Grenoble, France [4)] Philips, 850, rue J.Monnet, BP. 16, 38921 Crolles, France

**1. Introduction**

Thanks to its perfect channel electrostatic integrity, multi-gate transistor is the most promising solution to reach ITRS specifications for the 32nm node and below [1]. Many technologies have been proposed (FINFET [2-5], Tri-Gate [6], GAA-SON [7], MBCFET[8]). We already reported in a previous work a planar design adapted Gate All Around (GAA) MOSFET [9], signifying that bulk design was kept unchanged. Thanks to a new integration scheme, we report here a design adapted planar GAA with self aligned gates (SADAGAA). For the first time, the device associates two stacked channels with the ability to control each one with adjusted implants. Utilizing SON technology, we achieve thin films, and MESA-like isolation. Moreover, our new integration scheme brings the ability to co-integrate GAA MOSFET with SOI devices on the same wafer.

**2. Device Fabrication**

Both PDSOI and FDSOI substrates are suitable for our 2D co-integration. As described in fig.1., SOI layer can be processed as a single SOI device (2DSOI), as well as a bottom channel (BSOI) under GAA one. SADAGAA integration scheme is described fig.2. The first step is a multi-stack SiGe/Si/SiGe epitaxial growth on a (100) SOI substrate (a). The silicon layer thickness will determine the future thickness of the GAA channel. After having deposited a nitride hard mask, the whole stack is patterned with the GAA gate layer (b), stopping etch in the SOI layer (no lithography has to be done on the 2DSOI device). Since the SiGe layers are sacrifial ones, and will be replaced later with gate material, this operation results with the self alignment of the top and the bottom gates. Then source and drain are formed with a selective mono-crystal silicon epitaxy (c). (111) facets are obtained on nitride hard mask. In the next step, thanks to facets orientation high reproducibility, rigorous arsenic source and drain implantations can be performed, using tilted process at right angles with respect to the facets (about 55°). Active lithography is then performed, and the entire stack is etched down to the box (d). This step has two mains objectives: to obtain MESA-like isolation, and to open laterally on the SiGe layers. Thus, thanks to SON process [10], the two sacrificial SiGe layers can be etched selectively in respect with silicon (e). The remaining silicon film corresponds to our future channel, and presents excellent morphology as shown in fig.3. A 20A gate oxide is then thermally grown, and N+ poly-silicon is deposited. Thus, tunnels are filled with gate material. Next, a second gate etching for both SADAGAA (f) and 2DSOI devices are performed. This step aims at connecting laterally the two tunnels with gate material for SADAGAA device, and simply form gate for 2DSOI transistors. After having formed spacers, nickel silicide is done. End of the process is standard. Fig.4 illustrates the high level integration density potential of our device, showing SADAGAA in its standard circuit layout. TEM views (fig.5, fig.6) demonstrate the excellent morphology of the device: the channel thicknesses are 9.7nm for the GAA channel, and 27nm for the BSOI one.

**3. Results and discussion**

In this part, we focus on the way to get free of any negative impact of the BSOI channel on the device performance. Both GAA and BSOI channels are kept undoped. Considering its higher intrinsic threshold voltage, BSOI channel has no influence on the subthreshold behavior of a long channel SADAGAA device. But standard SOI short channel effects are not controlled as well as in a GAA channel. Therefore intrinsic threshold voltage of BSOI channel dramatically decreases with gate length. Fig.7. shows hump effect measured on a 45 nm gate length device, and is compared with an ideal characteristic obtained with a positive variation of Vt(BSOI). Indeed, a negative bias Vb applied on the backside of the wafer induces a threshold voltage shift of the BSOI channel (due to potential modification in the BSOI channel) without having any effect on the GAA channel. Permanent Vt(BSOI) shift can be achieved with preliminary implants in the SOI layer. Here we performed a boron pockets implantation near the BSOI channel. Fig.8. illustrates the near ideal subthreshold slope resulting from those pockets implants. Adjusted implants make possible to control each channel of our SADAGAA device. Fig.9. shows Vt MASTAR modeling for these three cases: 25nm SOI channel thickness with and without pocket implants, and 10 nm channel thickness for a GAA device. We demonstrate BSOI has no effect under the threshold for device down to 50nm gate length when pockets are implanted.

Thus pockets implants make possible to obtain excellent characteristics for our SADAGAA architecture. Fig.10 illustrates this statement. A 45nm gate length device has been measured with excellent DIBL and subthreshold slope (respectively 25mV/V and 69mV/dec). Because of the high coupling effects inherent to a GAA device, and to undoped channel, natural threshold voltage of the device is very low. Therefore, Ioff and Ion current are taken at Vg=-0.5V and Vg=0.7V respectively, simulating a TiN midgap gate. Current being normalized per active width, very good Ion/Ioff ratio is obtained, Ion=654µA/µm, Ioff=50pA/µm at Vd=1.2V. Fig.11.and fig 12. show excellent immunity of the device to short channel effects.

**4.Perspectives**

Our SON process based technology, combining mono-crystalline epitaxy with high selectivity plasma etching process results in a 3D-built device, with two stacked channels. With adjusted implantations we achieved here to control each one. With independently driven gates [11] promising multi-applications device can be envisaged. Even with common source and drain for both channels, a logic application could be addressed to the high performance top GAA channel, and a 1T-DRAM embedded memory function could be applied to the BSOI one [12].

**5.Conclusion**

We report here main results: First, a novel planar SADAGAA device has been presented with excellent short channel immunity due to its ultra thin film. Moreover we demonstrate its high level integration potential: the bulk layout is kept unchanged, we can co-integrate the SADAGAA with simple gate SOI transistor, and we achieved to control each channel of the 3D-built device.

**Acknowledgement**

This work was supported by the European project PULLNANO.

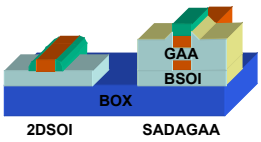



*Fig.1: Nomenclature of the 2D co-integration.*

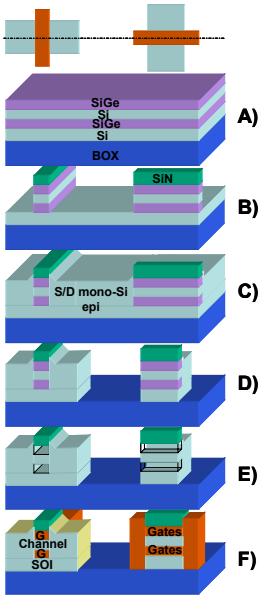



*Fig.2: Integration scheme of the SADAGAA device.*

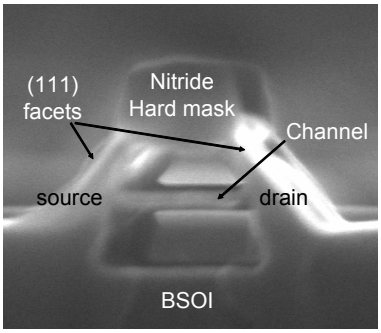



*Fig.3: View of the SADAGAA after SiGe selective etch (fig.1.e).*

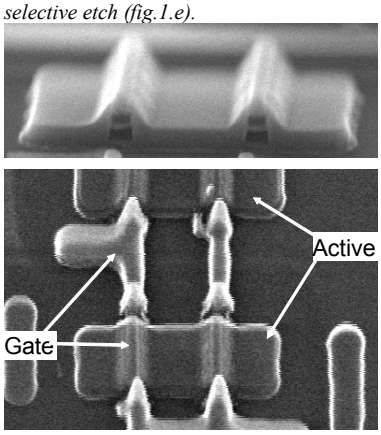
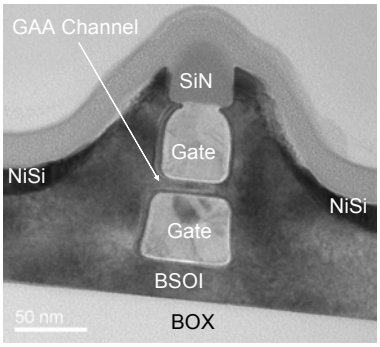



*Fig.4: Bulk layout is unchanged : view of a circuit after SiGe etch (see fig.1.e) and after second gate etch (see fig.1.f).*



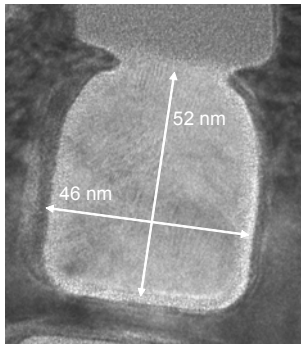
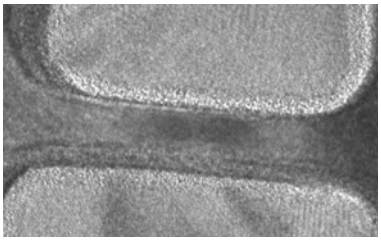




*Fig.5: TEM view of a 46 nm gate length SADAGAA device*



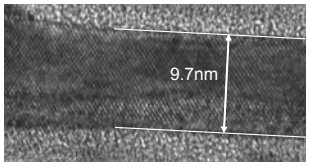



*Fig.6: Thanks to SON technology, ultra thin conduction channel is achieved (9.7nm).*

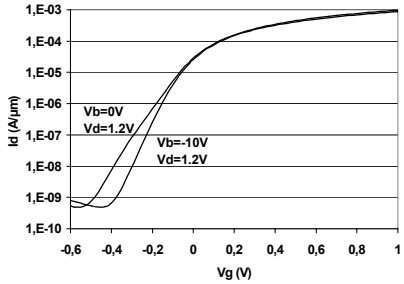



*Fig.7 Hump effect due lo a low BSOI threshold voltage for a 45nm gate length device.*

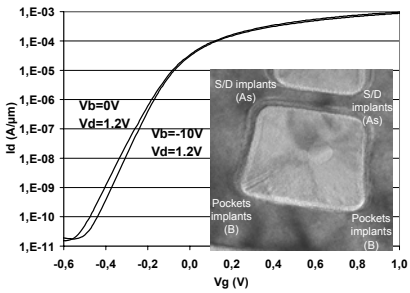



*Fig.8: Id(Vg) curve is near ideal when pockets implants are done in the BSOI channel.*

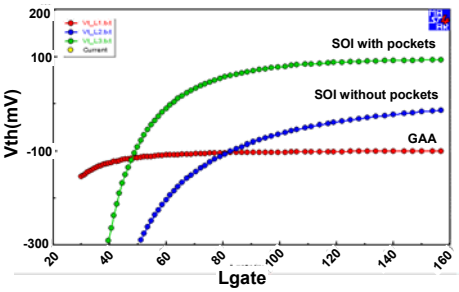



*Fig.9: MASTAR modeling of Vt roll-off of a GAA device with 10nm film (red), SOI device with 25nm channel thickness, with (green) and without (blue) pockets implants. Channels are undoped, gate is poly N+.*

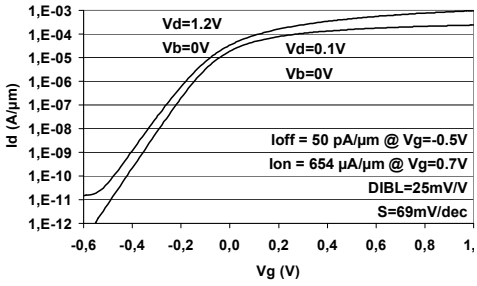



*Fig.10: Id(Vg) characteristics for a 46nm gate length SADAGAA NMOS with pockets implants and Vb=0V.*

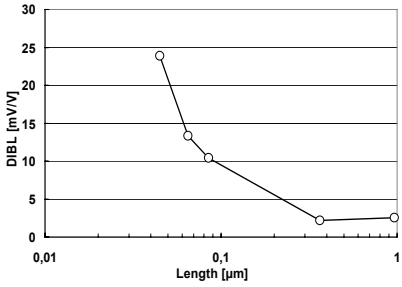



*Fig.11: DIBL (L). Excellent immunity to short channel effects are due to very thin film*

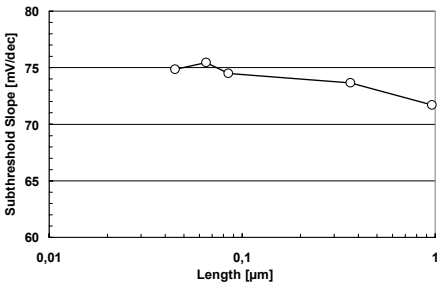



*Fig.12: Subthreshold slope as a function of gate length.*

## References:


[1] International Technology Roadmap for Semiconductors 2005.
[2] Y-K.Choi et al, IEDM Tech.Dig. , 2001, p.421
[3] B.Yu et al, IEDM Tech.Dig. , 2002, p.251
[4] J.Kedzierski et al, IEDM Tech Dig. , 2002, p247
[5] S.M.Kim et al, IEDM Tech Dig, 2004, p639
[6] K.W.Guarini et al, IEDM Tech.Dig. , 2001, p.425
[7] S.Harrison et al., IEDM Tech Dig, 2003, p449
[8] S.Y Lee, Symp VLSI tech 2004, p. 200
[9] R.Cerutti et al., SNW Tech Dig 2005, p12
[10] S.Monfray et al., IEDM Tech 2001, p645
[11] L.Mathew et al, VLSI Tech Digest 2005, p200
[12] R.Ranica et al, IEDM Tech Dig 2004, p277