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P-3-2

Monte Carlo Simulation of Band-to-band Tunneling in Silicon Devices

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1. Introduction

Band-to-band tunneling (BTBT) has attracted tremendous attention as a crucial reason for Gate-Induced-Drain-Leakage (GIDL) and hot-hole-injection (HHI), both, theoretically and experimentally [1-4]. However, up to date, many simulation studies are based on the Drift-Diffusion (DD) or Hydrodynamics (HD) model as a generation-recombination term which is not suitable to the nano-scale MOSFETs in which non-equilibrium transport is dominant. In this work, we include the BTBT in ensemble full-band Monte Carlo simulation and the band-trap-band (BTB) tunneling is also considered. The results are verified by comparing the pn junction reverse current with the experimental data. GIDL currents caused by BTBT in parallel with Si/SiO_2 interface and normal to Si/SiO_2 interface in a 45-nm channel-length Si nMOSFET have been investigated.

2. Simulation Method

The 2D ensemble full-band Monte Carlo (FBMC) device simulator developed in-house, described in [5], [6], is used. The acoustic and optical phonon scattering, the ionized impurity scattering, the impact ionization scattering and surface roughness scattering are taken into account. Fig.1 shows the BTBT mechanisms including band-trap-band (BTB) tunneling [1] included in our Monte Carlo simulation. For each time step, particle with charge P_c calculated by the equations (1)-(3) [7] will be generated in the BTBT region.

$$P_c = R_{BTBT} \cdot \Delta S \cdot \Delta t \tag{1}$$

$$R_{BTBT} = AD(E_{fn}, E_{fp})\varepsilon^2 \exp(-B/\varepsilon) \tag{2}$$

$$\begin{aligned} D(E_{fn}, E_{fp}) = {} & 1/(\exp[(E_i(x) - E_{fn}(x))/K_B T] + 1) \\ & - 1/(\exp[(E_i(x) - E_{fp}(x))/K_B T] + 1) \end{aligned} \tag{3}$$

where R_{BTBT} is the BTBT rate, ΔS is the area, A is a constant, $D(E_{fn},E_{fp})$ is net-rate factor, ε is local electric field, and B is the characteristic electric field. For the tunneling assisted by trap levels in the gap of the silicon, A and B are proportional to trap density of states/valence band density of states and $((E_g-E_T)/E_g)^{3/2}$ [4], respectively. The net-rate factor $D(E_{fn},E_{fp})$ and the BTBT rate of a pn junction are shown in Fig.2. The BTBT region can be automatically described by net-rate factor $D(E_{fn},E_{fp})$. Fig.3 shows the distribution of carriers density generated by BTBT. The results are verified by comparing the pn junction reverse current with the experimental data [8] shown in Fig.4. From the figure it can be seen that good agreement to the experimental data is achieved.

3. Simulation Results and Discussions

GIDL currents have been investigated in 45-nm-length Si nMOSFET with S/D extension as shown in Fig.5. It is assumed that the interface trap distribution has peaks at 0.05 eV above the center of the indirect gap [4], and the density of these interface traps is approximately $5x10^{16}$ cm^{-3} [4].The simulated distribution of electron and hole densities caused by BTBT are plotted in Figs. 6 and 7. It can be seen that the electron and hole generated by BTBT are assembled in the drain and channel region, respectively. Fig. 8 shows the average energy distribution of carriers drift and BTBT along the channel near the Si/SiO_2 interface. The BTBT carriers (especially the hole) energy is much higher than the common carriers' which will cause a crucial reliability issue. The GIDL currents caused by BTBT in parallel with Si/SiO_2 interface and normal to Si/SiO_2 interface as a function of drain voltage are shown in Fig.9. These are the first reported GIDL currents by using ensemble FBMC simulation. The results indicate the GIDL currents caused by BTBT in parallel with Si/SiO_2 interface is much more sensitive to the drain voltage. Except causing large leakage current, this current will have serious impact on the reliability of nano scale MOSFETs.

4. Conclusions

We included the BTBT in ensemble FBMC device simulator. The BTBT carriers density and energy distributions in a 45-nm channel-length Si nMOSFET have been investigated in detail. The simulation results indicate that the BTBT can cause additional hot carriers (especially hole) which should be pay more attention from the view point of reliability. Moreover, the GIDL currents caused by BTBT in parallel with Si/SiO_2 interface has a much stronger relationship with drain voltage compared with that caused by BTBT normal to Si/SiO_2 interface.

Acknowledgments

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References

[1] J. C. Guo, et.al., *IEEE TED*, **45** (1998) 1518. [2] T. H. Wang, et.al., *IEEE EDL*, **16** (1995) 566. [3] T. E. Chang, et.al., *IEEE TED*, **42** (1995) 738. [4] V. Nathan, et.al., *IEEE TED*, **40** (1993) 1888. [5] G. Du, et.al., *IEEE TED*, **52** (2005) 2258.[6] Z. L. Xia, et.al., *Solid State Electronics*, **49** (2005) 1942. [7] K. R. Kim, et,al., *International Conference on Simulation of Semiconductor Process and Devices* (2005) 159. [8] G. A. M. Hurkx, et.al., *IEEE TED*, **39** (1992) 331.

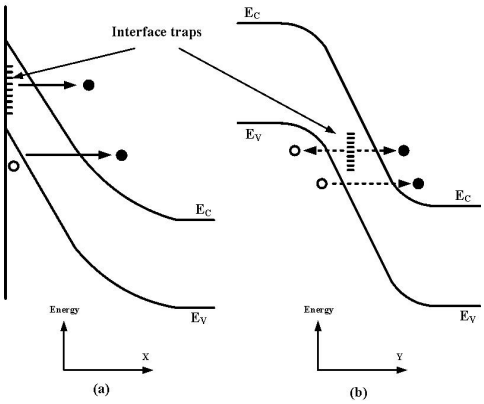

Fig.1 BTBT mechanisms including band-trap-band tunneling in nMOSFETs under deep depletion: (a) normal to Si/SiO_2 interface (b) in parallel with Si/SiO_2 interface.

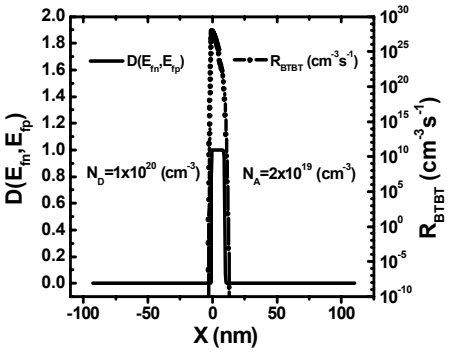

Fig.2 Net-rate factor $D(E_{fn},E_{fp})$ and band-to-band tunneling rate in a PN junction.

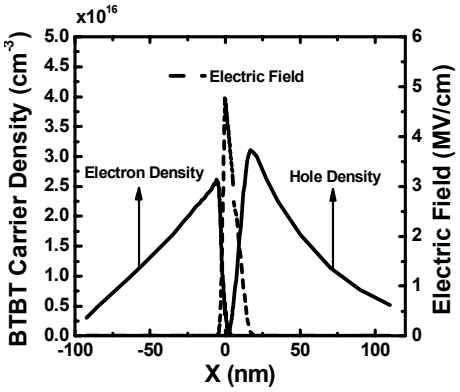

Fig.3 Band-to-band tunneling carrier density and electric field in a PN junction.

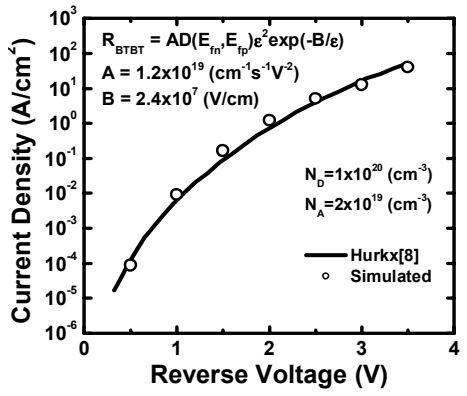

Fig.4 Simulated current density as a function of reverse voltage. For comparison, the measurement results [8] are also shown.

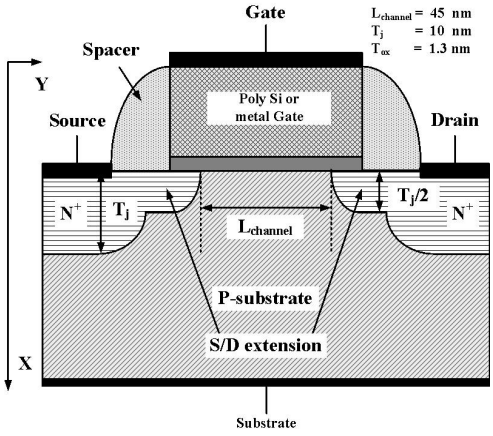

Fig.5 Schematic of a 45-nm channel-length Si nMOSFET with S/D extention.

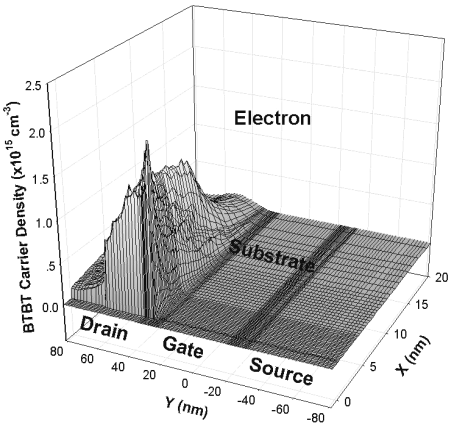

Fig.6 BTBT electron density distribution in a 45-nm channel-length Si nMOSFET.

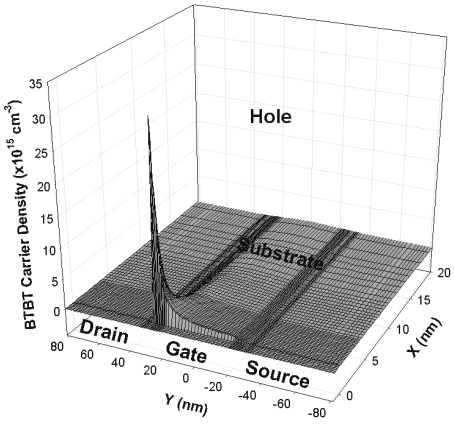

Fig.7 BTBT hole density distribution in a 45-nm channel-length Si nMOSFET.

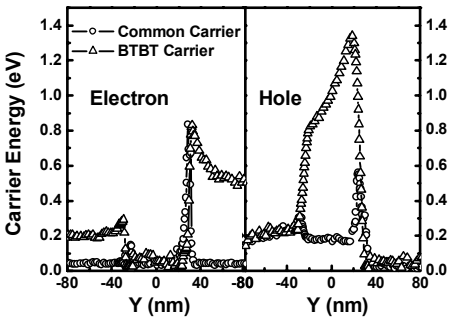

Fig.8 BTBT carrier average energy distribution along the channel near the Si/SiO_2 interface.

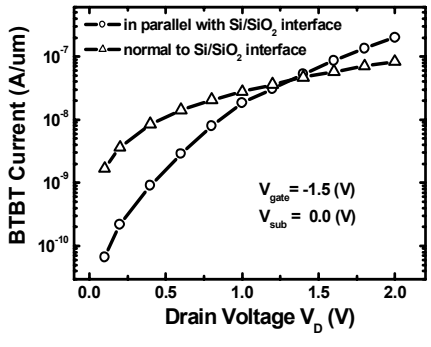

Fig.9 BTBT currents in parallel with Si/SiO_2 interface and normal to Si/SiO_2 interface as a function of drain voltage.