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N-Type Extended Drain Silicon Controlled Rectifier ESD Protection Device with High Latchup Immunity for High Voltage Operating I/O Application

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1. Introduction

Stable electrostatic discharge (ESD) protection is hardly realized in the high voltage operating double diffused drain N-type MOSFET (DDDNMOS) devices. This is due to the non-uniform current flow within these devices. Extremely strong snapback characteristics induce current crowding and consequential melting damages [1]. Thus self-protection using the DDDNMOS device is practically impossible and alternative approaches must be searched. Among various ESD protection devices, high voltage operating silicon controlled rectifier (SCR) can be an attractive candidate. However, the SCR device is very vulnerable to the latchup during the normal operation. Extensive works have been devoted to solve the problem, however ended with only limited successes. In this work, the so called, N-type extended drain silicon controlled rectifier (NEDSCR) device is suggested for high voltage I/O applications. It will be shown that the NEDSCR device can be well-equipped with both the excellent ESD protection performance and the high latchup immunity with proper junction / channel engineering.

2. Device description and simulation methodology

The NEDSCR device is constructed based on the DDDNMOS device with extended drain structure (i.e. non-adjacency of the drain N+ diffusion from the gate); the P+ diffusion is inserted into the N-Drift region on the drain side to form a part of anode electrode (Fig. 1). The resulting structure becomes a high voltage operating SCR device consisting of a lateral NPN bipolar junction transistor (BJT) and vertical PNP BJT. For the ESD application, the anode is connected to each I/O pad (or to Vdd power pad) while the cathode is connected to Vss ground pad.

The conventional NEDSCR_Std device is based on normal DDDNMOS device without modification on the junction / channel region. In the modified NEDSCR_CPS device, the P-type counter pocket source (CPS) implant is added to enclose the cathode N+ diffusion. The CPS implant dose and energy can be varied centering on the N-Drift implant condition. Thus the junction / channel profile is modified. Moreover, effective P-type doping outside the cathode N+ diffusion is drastically changed. The overlap margin of anode N+ diffusion over N-Drift region (*'S'* in Fig. 1) is either kept same with that of NEDSCR_Std, or made smaller.

3. Results and Discussion

Characteristics of the NEDSCR devices are investigated using thermal incorporated 2-dimensional simulations. Devices were fabricated using TSUPREM4 (Synopsis Co.) process simulator following MagnaChip's high voltage (*Vop* ≈ 30V) process. Device characteristics were analyzed using DESSIS device simulator. The transient simulations were performed adopting ladder type current pulses with rise time 10nsec and duration 100nsec.

Simulation deduced *I-V* relation of the NEDSCR_Std clearly shows typical SCR-like characteristics (Fig. 2). It demonstrates extremely low snapback holding voltage (*Vh*) and low on-resistance (*Ron*). The *Vh* is much smaller than the *Vop*. This implies that the NEDSCR_Std device, when used as a power clamp ESD protection device between Vdd and Vss, becomes very vulnerable to latchup problem during normal operation. Different from the NEDSCR_Std device, the NEDSCR_CPS devices are characterized by high *Vh* and high *Ron*. The *Vh* is shown to be higher than *Vop*. Thus, the latchup immunity is guaranteed. The off-state leakage current of the NEDSCR_CPS device decreases by almost 4 orders due to the CPS implant. Current immunity level of the NEDSCR_CPS device decrease down upon modification. However it is still high enough for area-efficient ESD protection performance. Current capacity of the NEDSCR_CPS device is estimated as about ≈3A for device width 100um. The *I-V* characteristics are strongly dependent on the parameter *'S'*. Reduction of the parameter *'S'* results in the shrinkage of the effective base width between the two electrodes. This result in a little smaller triggering voltage and lower *Vh*, which guarantees more flexibility in the optimization for ideal ESD protection performance.

Corresponding contour data provide phenomenological explanation on the drastic change of the *I-V* relations (Fig. 3). At the BJT triggering point, the depletion induced high electric field region is formed along the N-Drift / HP-Well border. This is qualitatively same regardless of the device type (refer (A) and (D)). However, when the NEDSCR_Std enters the snapback holding point or higher current region (refer (B) and (C)), the high electron injection from the cathode N+ diffusion leads to the deep electron channeling under the gate. That is, the background doping of the HP-Well and the N-Drift region is completely screened by the injected free carriers. Thus, the whole current path between the cathode and the anode becomes field-free, as explicitly shown in the corresponding electric field contour. The low *Vh* and low *Ron* can be explained in terms of the field-free and wide current path between two electrodes. High electron injection induced base push out (or Kirk effects) and the consequential low *Vh* and the low *Ron* had been addressed in the precedent works [2, 3].

Talking on the contour data of the NEDSCR_CPS device, due to CPS implant, the lateral directional high electric field region still survives even at the snapback holding or at higher current level. Moreover, the CPS implant introduces more resistive path between the cathode and the anode. Thus, the *I-V* characteristics with high *Vh* and the high *Ron* appears as shown in Fig. 2.

4. Conclusions

The, so called, NEDSCR_CPS device demonstrates both the robust ESD protection characteristics and high latchup immunity. The counter pocket source implant and the overlap margin of the

anode N+ diffusion over the N-Drift are critical factors in the amendment engineering. In conclusion, the NEDSCR_CPS device can be a promising ESD protection device for high voltage I/O applications.

Acknowledgements

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References

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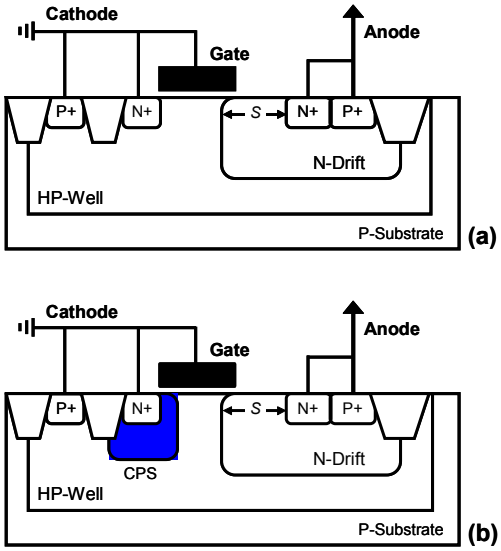

Fig. 1. Schematic diagram of high voltage operating (a) NEDSCR_Std device and (b) NEDSCR_CPS device.

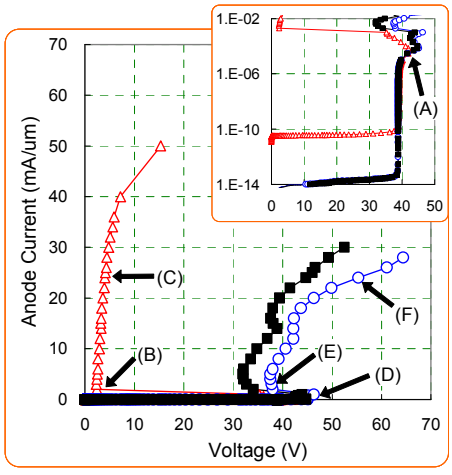

Fig. 2. Simulation results on *I-V* relations for NEDSCR devices (open triangle Δ for NEDSCR_Std with S = 1.6um, open circle ○ for NEDSCR_CPS with S = 1.6um, closed square ■ for NEDSCR_ CPS with S = 1.0um). Graphs in the inset represent same *I-V* relations with y-axis on log scale.

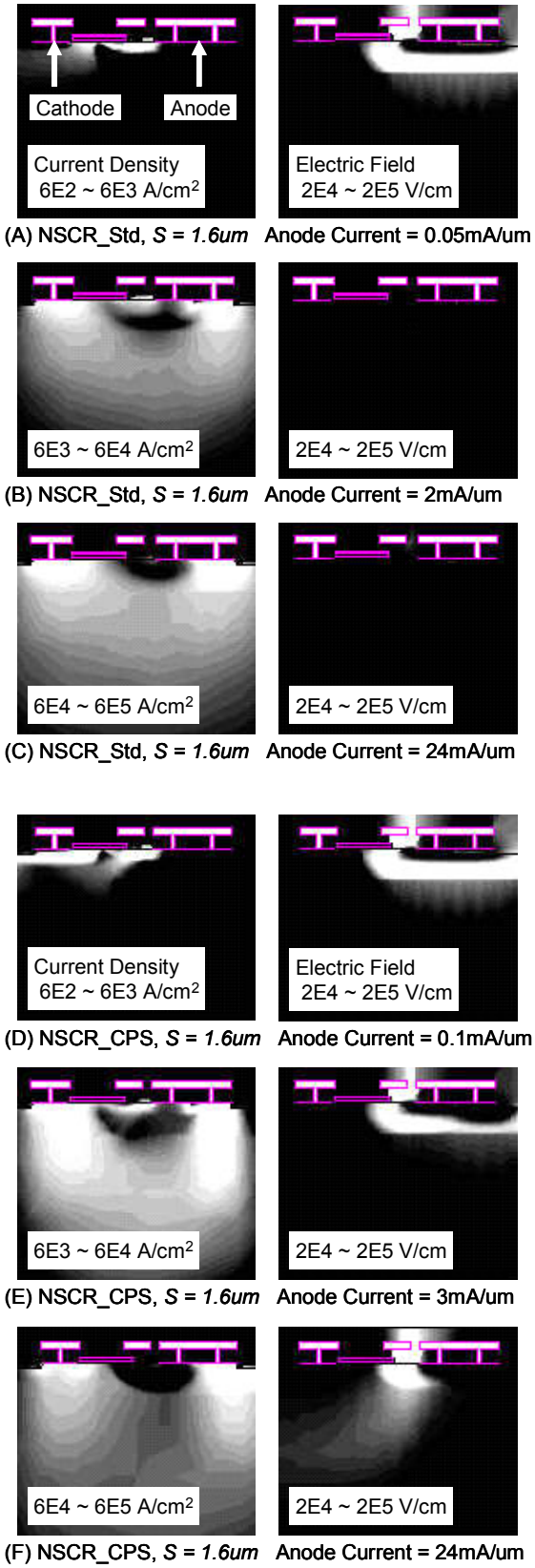

Fig. 3. Contour data of current density and electric field at the triggering point (A, D), at the snapback holding point (B, E) and at the high current region near thermal breakdown point (C, F). Contours at (A, B, (C) represent for the NEDSCR_Std (S = 1.6um) device and those at (D, E, F) represents for NEDSCR_CPS (S = 1.6um) device.