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Strain Efficiency Enhancement with Stress Intermedium Engineering (SIE) for Sub-65nm CMOS Scaling

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Abstract

Performance gain arising from 40nm/0.7GPa tensile contact-etch-stop layer has been significantly amplified from intrinsic 6% up to 15% by newly developed Stress Intermedium Engineering (SIE) technology. A stress transfer model considering mechanical properties of intermedium materials is proposed to account for the performance boost. Neither worse short-channel effects nor abnormal junction leakage were found with the SIE technology. Excellent gate oxide integrity and hot carrier immunity of the SIE technology have also been verified for manufacture implementation. This study features a new paradigm of channel strain engineering for sub-65nm CMOS scaling, in addition to conventional approach of stressor optimization.

Introduction

Using contact-etch-stop layer (CESL) as a stressor to strain silicon channel for higher drive current is at present the simplest and the most widely adopted strained-Si technology [1-2]. Theoretically, the induced channel strain will be increased with increasing the CESL stressor intensity and/or thickness [3-6]. However, the stressor thickness is usually limited by design rule, and even has to be reduced with device feature size scaling down. The stressor intensity is also limited by process available, from manufacture viewpoint. Under these boundary conditions, the efficiency of stress intermedium (between aforementioned stressor and the target strained channel, shown in Fig. 1) is then worth our while to explore, for fully utilizing the adopted stressor strength. So far, to the extent of our knowledge, there are no published literatures for such "stress intermedium" discussion. In this paper, our experiments including source/drain silicide engineering and junction profile modification for the stress intermedium optimization show that the CESL-stressor induced performance gain can be significantly amplified. Mechanical properties of the stress intermedium will be discussed for the first time.

Device Fabrication

A 65nm-gate N-MOSFET with 40nm/0.7GPa tensile CESL stressor was fabricated for the stress intermedium study. Gate spacer width and CESL stressor thickness is fixed in this work. Source/drain with Co silicide and Ni silicide are splitted for comparison. The silicide's and neighbor junction's profiles are optimized for minimum parasitic source/drain resistance while maintaining short-channel-effect control (i.e. the same subthreshold and junction leakage), and also for achieving maximum channel strain as so-called "stress intermedium engineering (SIE)".

Results and Discussions

● **Amplified Performance Enhancement with SIE.** Table 1 summarizes performance improvement percentages of various technologies: CESL stressor only, SIE only, and CESL stressor + SIE, over control devices. In both cases of Co silicide and Ni silicide, performance enhancement of "CESL stressor + SIE" is obviously larger than the sum of individual "CESL stressor only" and "SIE only". Fig. 2-4 show the detailed experimental data of each performance enhancement technology with Co silicide, and Fig. 5 shows that with Ni silicide. For $I_{d,sat}$ comparison, minor enhancement by SIE (2% for Co silicide case and 1.5% for Ni silicide case) significantly increases performance gain of CESL stressor (from 6% up to 15%, and from 4% up to 8%, for Co and Ni silicide, respectively). The SIE also increases $I_{d,lin}$, but not as much as for $I_{d,sat}$, from 11% up to 16%, and from 7% up to 9%, for Co and Ni silicide, respectively. The SIE itself in our experiments is originally designed for parasitic resistance (R_{ext}) reduction [7-8], which accounts for most of the $I_{d,lin}$ difference between "CESL stressor" and "CESL stressor + SIE", but not able to make up the much bigger $I_{d,sat}$ difference between them. A model concerning mechanical property of intermedium materials to account for different stress transfer efficiency is therefore proposed, as schematically illustrated in Fig. 7.

● **Stress Transfer Efficiency.** Table 2 and Fig. 7 show the mechanical property of intermedium materials and the schematic of stress transfer through stress intermedium, respectively. A channel stress (σ_{xx} and σ_{zz}) simulation is used to evaluate the stress transfer efficiency at different mechanical property of intermedium (Co silicide, Ni silicide, and Si), as shown in Fig. 8. An ideal stress intermedium should be able to generate higher tensile stress on channel direction (σ_{xx}) and higher compressive stress on vertical direction (σ_{zz}) for enhancing N-MOSFET drive current [9]. This is consistent with that SIE using Co silicide shows much higher performance gain than Ni silicide under the same CESL stressor (40nm/0.7GPa), due to Co silicide with lower Young's modulus gives rise to much higher compressive σ_{zz} at slightly degraded σ_{xx}. The more desired channel stress through engineered Co silicide and proper junction profile is herein expressed as arising from higher stress transfer efficiency with better stress intermedium.

● **SIE Device Characteristics.** The V_t roll-off characteristic of N-MOSFET with SIE and tensile CESL stressor is similar to control devices (Fig. 9). The Vt shift (~15mV) is due to band split by tensile strain. The I_D-V_G characteristic of a 65nm channel N-MOSFET device with SIE is shown in Fig.10. It is noticed that the subthreshold swing (100mV/dec) and leakage current (subthreshold leakage and GIDL) of the SIE assisted device are compatible to the control devices, indicating no side effects on the leakage current with optimized silicide and junction profile. The I_D-V_D output characteristics of the N-MOSFET device with SIE and tensile CESL stressor is shown in Fig. 11. Inversion thicknesses examination of gate oxide shows no difference between control, with SIE, and with tensile CESL + SIE (Fig. 12). Furthermore, the gate oxide integrity is not adversely affected with the SIE approach (Fig. 13). Finally, reliability test of hot carrier immunity (HCI) is also checked. Both SIE assisted and unstrained control show similar HCI lifetime (Fig. 14).

Conclusions

A novel Stress Intermedium Engineering technology has been developed to amplify CESL-stressor induced performance gain from 6% up to 15%. Excellent gate oxide integrity, hot carrier immunity, and also the same short-channel-effect control are achieved with this new technology. The technology enhances channel strain through stress intermedium optimization rather than increasing stressor intensity/thickness, thus is very promising for sub-65nm CMOS scaling.

References

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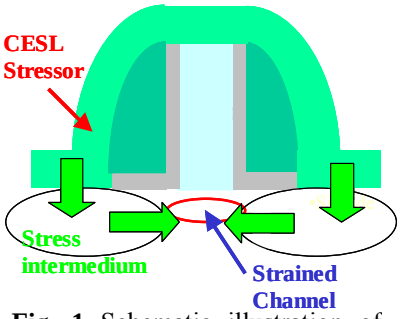
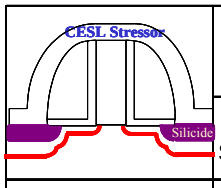


Fig. 1 Schematic illustration of the stress intermedium between CESL stressor and strained channel.

Table 1 Summary table of performance improvement percentage of various technologies.



	Performance Improvement	
	Co Silicide	Ni Silicide
CESL stressor only	6%	4%
SIE only	2%	1.5%
SIE + CESL	15%	8%

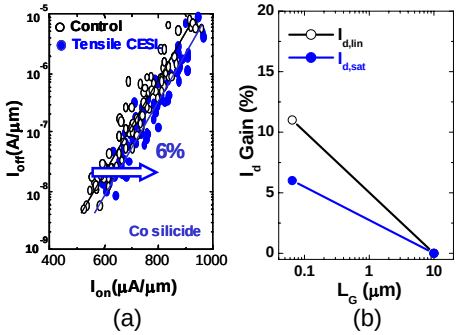


Fig. 2 NMOSFET performance with 40nm/0.7GPa tensile CESL stressor. (a) $I_{d,sat}$ gain 6%, and (b) $I_{d,lin}$ gain 11%.

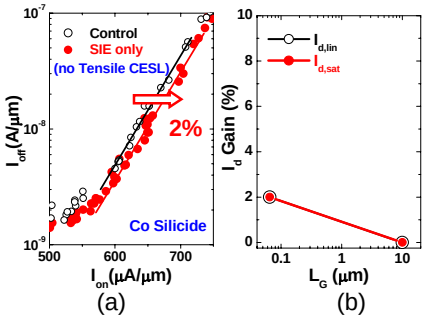


Fig. 3 Performance enhancement with SIE only. (a) 2% enhancement for $I_{d,sat}$, and (b) also 2% enhancement for $I_{d,lin}$.

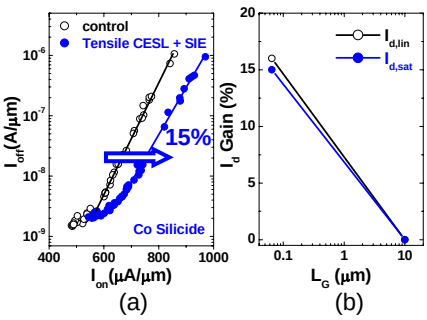


Fig. 4 Performance enhancement with tensile CESL stressor and SIE (Co silicide process). (a) 15% gain for $I_{d,sat}$, and (b) 16% gain for $I_{d,lin}$.

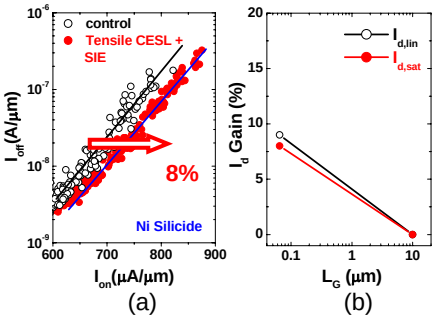


Fig. 5 Performance enhancement with tensile CESL stressor and SIE (Ni silicide process). (a) 8% enhancement for $I_{d,sat}$, and (b) 9% enhancement for $I_{d,lin}$.

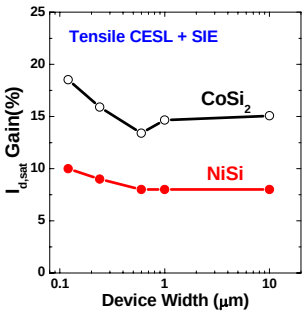


Fig. 6 More than 15% ($CoSi_2$) and 8% (NiSi) $I_{d,sat}$ gain with tensile CESL and SIE on all device widths.

Table 2 Summary table of mechanical property of stress intermedium materials.

Intermedium	Young's Modulus	Poisson Ratio (ν)
Si	187 Gpa	0.28
NiSi	132 Gpa	0.33
CoSi2	114 Gpa	0.33

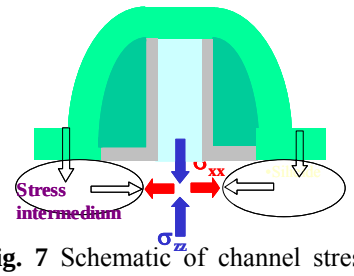


Fig. 7 Schematic of channel stress due to different SIE materials with tensile CESL.

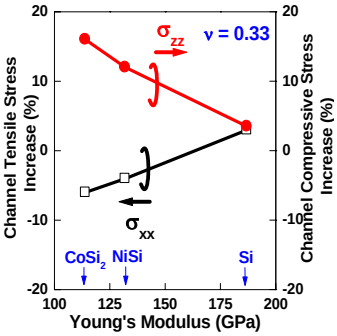


Fig. 8 Simulation of channel stress (σ_{xx} and σ_{zz}) vs. stress intermedium materials (keep Poisson Ratio = 0.33) under tensile CESL stressor.

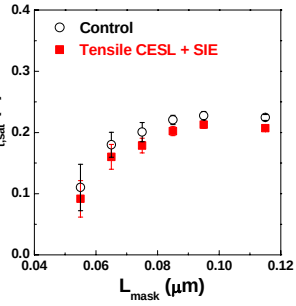


Fig. 9 Vt roll-off characteristics of N-MOSFET devices with SIE and tensile CESL stressor in comparison with control devices.

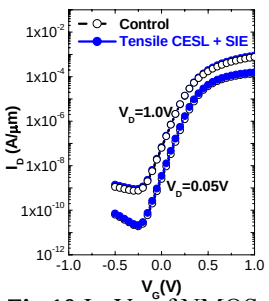


Fig.10 I_D-V_G of NMOS with SIE and tensile CESL.

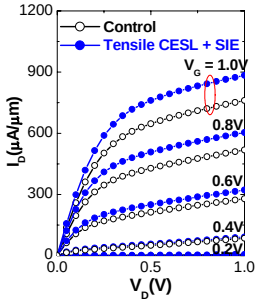


Fig.11 I_D-V_D of NMOS with SIE and tensile CESL.

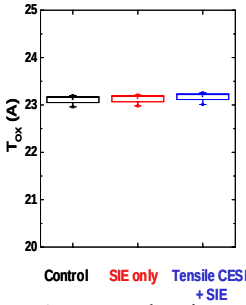


Fig. 12 The inversion thickness of gate oxide.

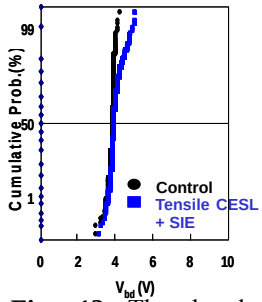


Fig. 13 The breakdown voltage on gate oxide integrity (GOI).

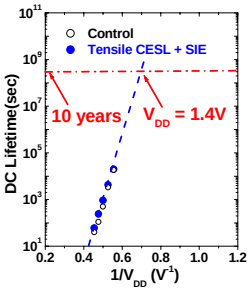


Fig. 14 Hot carrier lifetime of tensile CESL stressor + SIE.