

Empirical Model of Phonon-Limited Electron Mobility for Ultra-Thin Body SOI MOSFET

Tsuyoshi Yamamura, Shingo Sato, and Yasuhisa Omura

Graduate School of Eng, Kansai University, 3-3-35, Yamate-cho, Suita, Osaka 564-8680, Japan
Phone: +81-6-6368-1121 E-mail: omuray@ipcku.kansai-u.ac.jp

1. Introduction

The two-fluid density-gradient (2FDG) model has made it possible to obtain electron density in the two-fold and four-fold valleys without solving the Schrödinger equation [1]. However, to express the precise drain current (I_d) of MOSFETs more simply in device simulations, empirical mobility models for each valley are needed.

As the first step, we model phonon-limited electron mobility because electron-phonon interaction is a dominant scattering mechanism in a wide range of effective electric fields (E_{eff}) at room temperature; the scattering processes stemming from surface roughness (SR) or interface charges should be taken account of only at either very high or very low fields. As the SOI-layer thickness (T_{SOI}) decreases, the phonon-limited electron mobility (μ_{ph}) significantly varies [2, 3]. Calculations indicate that the variation is due to, in part, the quantum effect. Based on those results, we introduce an empirical model that involves a function of T_{SOI} and E_{eff} .

2. Device structure and simulations

The device structure assumed is the single-gate (SG) n-channel SOI MOSFET shown in Fig. 1. As shown in Fig. 1, gate oxide thickness is 3 [nm] and buried oxide thickness is 200 [nm]. Impurity concentrations (N_A) in the SOI-layer and Si substrate are taken to be 5×10^{15} [cm⁻³].

This article simulates the phonon-limited electron mobility in the (100) and (111) Si inversion layers in such ultra-thin body SOI MOSFETs at 300K using a relaxation time approximation based on 1-D self-consistent calculations. The physical parameters used in the calculation are listed in Tables 1 and 2.

3. Results and Discussions

We propose empirical models of phonon-limited mobility in the two-fold valley ($\mu_{ph,2fold}$) and in the four-fold valley ($\mu_{ph,4fold}$). Mobility model for (111) surface is not shown below to save description space.

3.1 Empirical Model of Phonon-Scattering-Limited Electron Mobility in the Two-Fold Valley: (001) surface

$$m_{ph,2fold} = AE_{eff}^2 - BE_{eff} + C, \quad (1)$$

$$A = \frac{a_1 b_1}{a_1 + b_1}, \quad B = \frac{a_2 b_2}{a_2 + b_2}, \quad C = \frac{a_3 b_3}{a_3 + b_3}, \quad (2a), (2b), (2c)$$

$$a_1 = 1.15 \exp\left[\frac{3(T_{SOI} + 4)}{4}\right] + 17, \quad (3a)$$

$$b_1 = -0.250875 \times T_{SOI} + 215.5, \quad (3b)$$

$$a_2 = 1.54 \exp(T_{SOI} + 3.5) + 19.0, \quad b_2 = 704.2 \quad (4a), (4b)$$

$$a_3 = 1.6 \exp[1.23(T_{SOI} + 3.5)] + 150.0, \quad b_3 = 1108, \quad (5a), (5b)$$

3.2 Empirical Model of Phonon-Scattering-Limited Electron Mobility in the Four-Fold Valley: (001) surface

$$m_{ph,4fold} = DE_{eff}^E, \quad (6)$$

$$D = \frac{a_4 b_4}{a_4 + b_4}, \quad E = \frac{abc}{ab+bc+ca}, \quad (7a), (7b)$$

$$a_4 = 1.15 \exp\left[\frac{(T_{SOI} + 3.3)}{1.1}\right] + 90, \quad b_4 = 414.14, \quad (8a), (8b)$$

$$a = -0.02546 \times T_{SOI} + 0.1, \quad b = -0.113, \quad (9a), (9b)$$

$$c = 0.0000028 \exp(2.3T_{SOI}), \quad (9c)$$

We draw the simulation results of phonon-limited electron mobility in the two-fold valley ($\mu_{ph,2fold}$) and in the four-fold valley ($\mu_{ph,4fold}$) and empirical models, which are shown with parameter of T_{SOI} in Fig. 2 and Fig. 3, respectively. In Fig. 4, we show T_{SOI} dependencies of phonon-limited electron mobility models of (001) and (111) surfaces for comparison. Empirical models for (001) and (111) surfaces accurately reproduce the simulation results such as E_{eff} dependence and T_{SOI} dependence.

When electric field along the channel is assumed to be uniform, drive current (I_d) is approximately expressed by the following equation (10).

$$I_d \approx \frac{W}{L} V_d (q m_{2fold} N_{2fold} + q m_{4fold} N_{4fold}), \quad (10)$$

where W is the channel width, L is the channel length, μ is the electron mobility, and N is the surface electron density; the subscripts "2fold" and "4fold" represent the two-fold valley and four-fold valley, respectively.

Using the electron density obtained from the 2FDG model and the empirical models (equations (1) and (6)), calculated I_d curves for (001) and (111) surfaces vs. gate voltage (V_g) is shown in Fig. 5 for $T_{SOI} = 5$ [nm]; here a metal gate is assumed. As shown in Fig. 5, entire I_d - V_g characteristics are successfully represented. However, the models don't reproduce TCAD simulation result [4], which suggests that the SR model must be included [3].

References

- [1] S. Sato and Y. Omura, *Jpn. J. Appl. Phys.*, vol. 45, No. 2, pp. 689-693, 2006.
- [2] M. Shoji and S. Horiguchi, *J. Appl. Phys.*, vol. 82, p. 6096, 1997.
- [3] S. Takagi et al., in *IEEE IEDM Tech. Dig.*, p. 219, 1997.
- [4] TCAD/DESSIS operation manual, ver. 7.5, Synopsis.

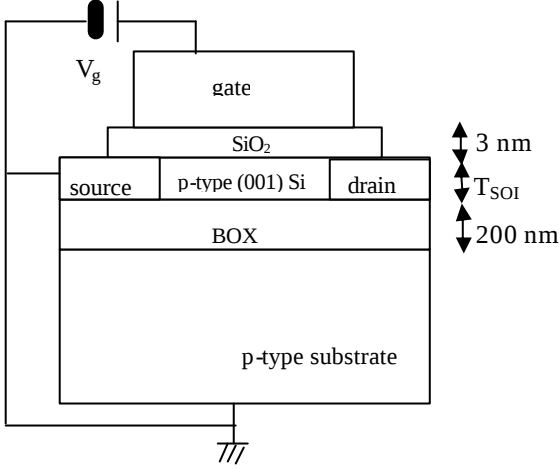


Fig. 1. Device structure considered.

Table. 1. Physical parameters used in the present calculations.

Parameters	Values [unit]
m_0	free electron mass 9.11×10^{-31} [kg]
m_l	longitudinal effective mass $0.98m_0$
m_t	transverse effective mass $0.19m_0$
m_{d2}	density-of-state mass in two-fold valley $0.19m_0$
m_{d4}	density-of-state mass in four-fold valley $0.43m_0$
m_{c2}	conductivity mass in twofold valley $0.19m_0$
m_{c4}	conductivity mass in fourfold valley $0.32m_0$
ρ	crystal density 2329 [kgm^{-3}]
S_1	sound velocity 9037 [ms^{-1}]
D_{ac}	acoustic deformation potential 12.0 [eV]

Table. 2. Parameters for inter-valley phonon scattering models.

Type of inter-valley Scattering	phonon energy E_k [meV]	deformation potential D_k [$\times 10^8$ eVcm $^{-1}$]
f	19.0	0.3
f	47.4	2.0
f	59.0	2.0
g	12.1	0.5
sg	18.5	0.8
bg	62.0	11.0

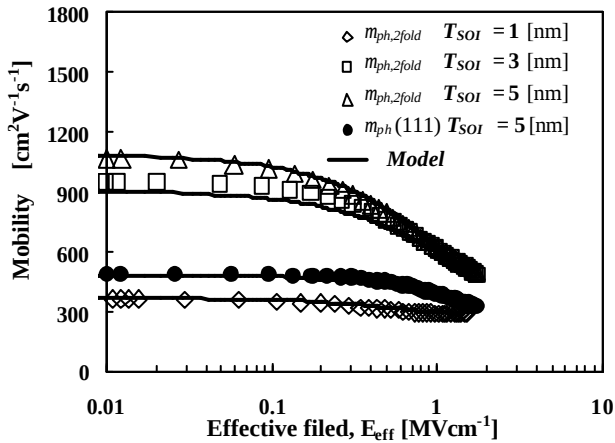


Fig. 2. E_{eff} dependence of phonon-limited electron mobility in the two-fold valley and in inversion layer on (111) surface.

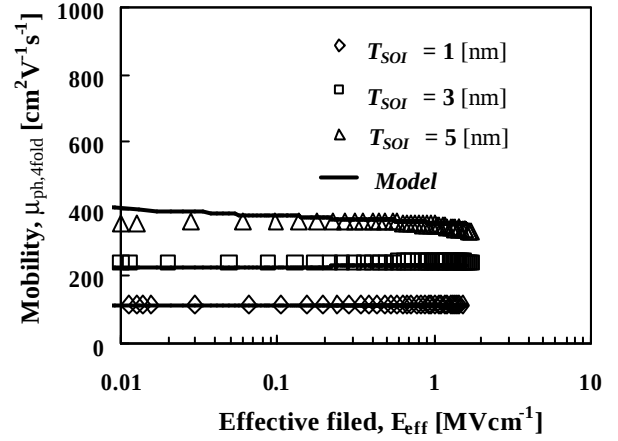


Fig. 3. E_{eff} dependence of phonon-limited electron mobility in the four-fold valley.

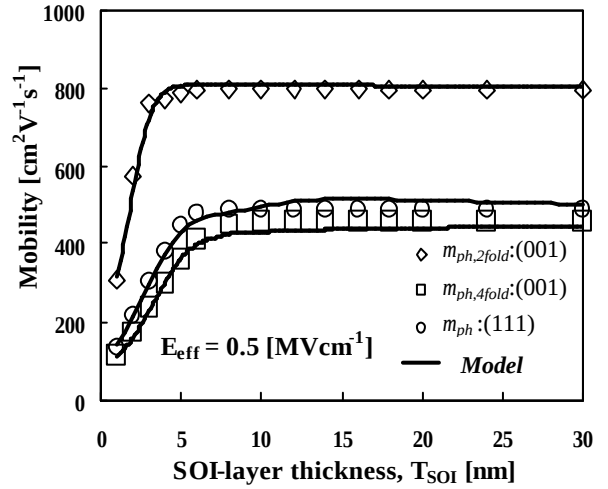


Fig. 4. T_{SOI} dependencies of phonon-limited electron mobility for (001) or (111) surface.

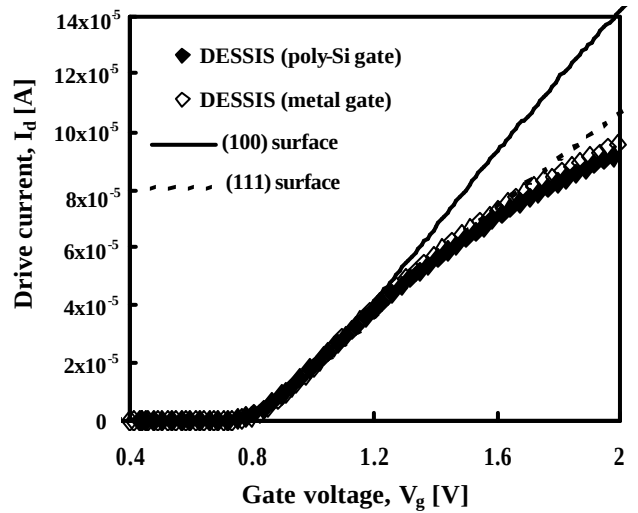


Fig. 5. Calculated I_d versus V_g in SOI MOSFETs with 20-nm thick SOI-layer. $L = 500$ [nm], $W = 1$ [μm], $V_a = 0.1$ [V]