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Re-examination of 1/f Noise in FD-SOI for Practical Usage of Analog Circuits

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1. Introduction

The silicon-on-insulator (SOI) CMOS technology which posseses the advantage of low power, high integration and low cost has proven its merits in RF/analog applications [1]. The floating body effect (FBE) in partially depleted (PD) SOI MOSFETs leads to kink in drain current characteristics. FBE also gives rise to excess low frequency noise in floating body PD devices (Fig. 1) [2]. Fully depleted (FD) SOI MOSFETs can provide sufficient control over short channel effects [3] and also have the improved low frequency noise because of the kink free characteristics. However FD-SOI also has excess noise issues because FD-SOI turns to be PD-like to achieve low leakage current. Recently non-doped/no-overlap FD SOI with reverse polarity gate (p-type polysilicon gate for NMOS) is reported (Fig. 2) [4]. FD SOI is also suitable for preparing a intrinsic depletion mode MOS (DMOS). In this paper, we examined the 1/f noise of bulk, floating body SOI with normal polarity gate (n-type polysilicon gate for NMOS) and reverese polarity gate, and SOI DMOS with normal polarity gate first time. The temperature dependence of 1/f noise of these devices is also studied. The analog bias condition (VGT(Vgs-Vth)=0.15V) is used for the measurements of 1/f noise.

2. Experimental

The devices investigated are FD SOI n-MOSFETs (with normal and reverse polarity gate) and SOI DMOS processed in a 0.15μm technology on 200mm UNIBOND wafers. The final Si thickness is 40nm and the buried oxide thickness 200nm. The bulk devices are also processed in a 0.15μm technology. The gate dielectric of all devices consists of a 6.5 nm NO oxide and a 150 nm polysilicon layer. We evaluate I/O transistors because analog is typically implemented on I/O transistors. All devices have gate length 1 μm and gate width 10μm. The noise spectral density was measured in the frequency range of 10 Hz to 100kHz.

3. Results and Discussion

In Fig. 1 excess noise is not observable in curve #1 or curve #2. Lorentzian noise is significant when the drain bias is around the kink onset voltage.Therefore from view point of practical usage of analog cricuits, bias condition around Gm peak (Vdrive is around 0.15V) is imporatant and there is no Lorentzian noise for this condition. Fig. 3 shows that FD SOI is also suitable for DMOS with low carrier concentration which is a limit in bulk MOSFETs due to well implantation. In bulk DMOS, it is difficult to control the short channel effects, however FD-SOI has better control of these because of thin Si film and buried oxide structure. The bias condition for the measurements is VGT=VDS which is used in cascode circuits shown in Fig.4. It is typical analog configuration. Fig.5 shows the gate overdrive dependence of gate noise power in bulk, floating body SOI with normal polarity gate (BF_Normal in Figs.) and with reverse polarity gate (BF_Reverse in Figs.), and SOI DMOS with normal polarity gate. It can be seen that there is no gate bias dependence in SOI DMOS and BF_Reverse. However bulk devices show some gate bias dependence espesially in low gate bias region. The comaparison of the gate noise power for different devices at room temperature and 125°C is shown in Fig.6. It is clear from the figure that noise performance of DMOS and floating body SOI with reverse polarity gate is suprior among these devices at room temperature as well as at T=125°C. Fig.7 shows the temperature dependence of gate noise power in bulk and SOI DMOS. In bulk devices noise increases with the temperature however change is very small for SOI DMOS. The increase in the noise of bulk devices at high temperature is due to temperature dpendence of Vt. Temperature dependence of Vt of all four devices is shown in Fig. 8. The Vt of bulk devices decreases with the increase in temperature. However the change in Vt of SOI DMOS is small with temperature. The gate bias for T=125°C is smaller than that of T=25°C for the same VGT because of the Vt difference. And from Fig. 5, noise in bulk devices increases with the decrease of gate bias hence the noise at T=125°C is larger than that of T=25°C.

4. Conclusion

The 1/f noise of the bulk, floating body SOI with normal polarity gate, DMOS with normal polarity gate and and floating body SOI with reverse polarity gate devices is investigated. We focused on practical bias conditions. It is found that 1/f noise of FD SOI with reverse polarity gate and DMOS is better than that of the other devices especially low Vdd region. It is also found that DMOS and FD SOI with reverse polarity gate show the lower 1/f noise even at higher temperatures. Therefore using FD-SOI DMOS we can achieve superior analog performance.

References

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[2] W. Jin et. al., IEEE Trans. Electron Devices, 46 (1999) 1180.
[3] B. Doris et al. in IEDM Tech. Dig. (2002) 267.
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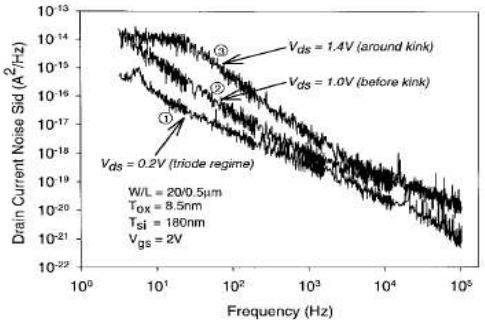
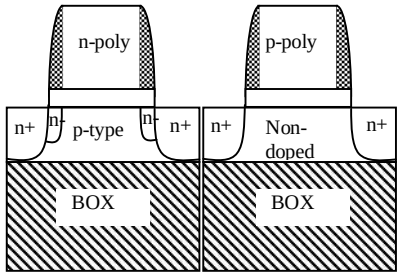
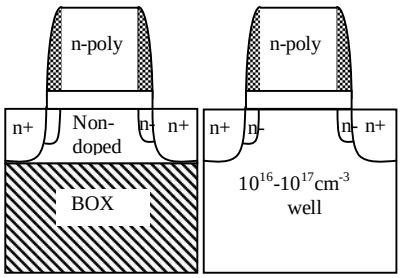


Fig. 1. Low frequency noise spectra before and around kink [2].



(a) (b)

Fig. 2. Structure of floating body SOI with (a) normal polarity gate (b) and reverse polarity gate



(a) (b)

Fig. 3. Structure of (a) SOI DMOS (b) Bulk DMOS

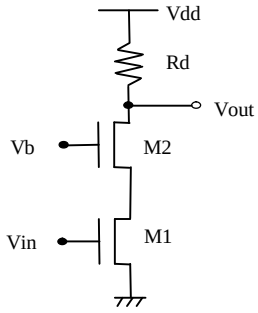


Fig. 4. Cascode circuit

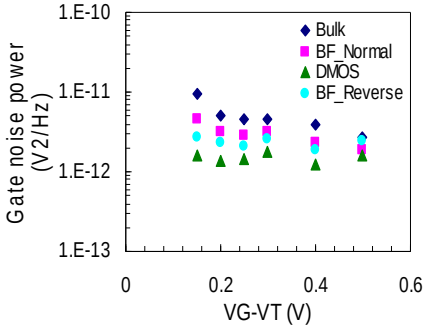


Fig. 5. Gate overdrive dependence of gate noise power in different structures.

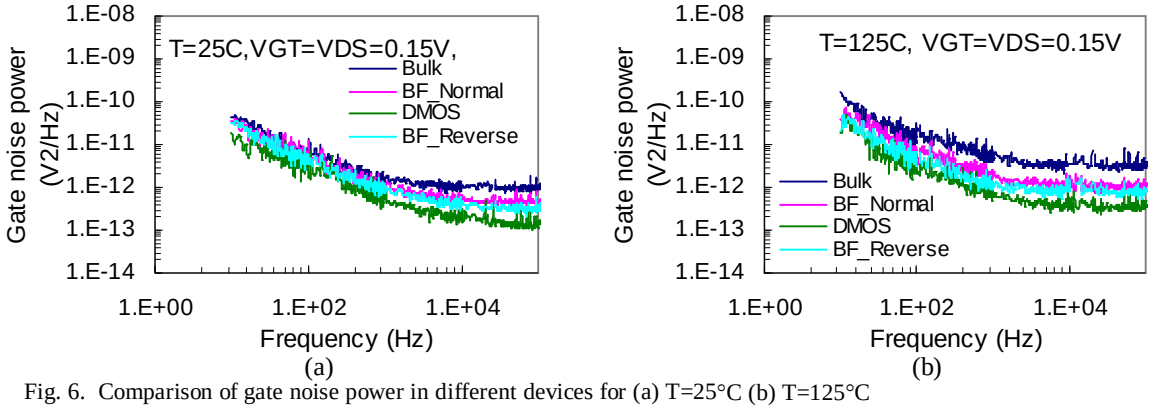


Fig. 6. Comparison of gate noise power in different devices for (a) T=25°C (b) T=125°C

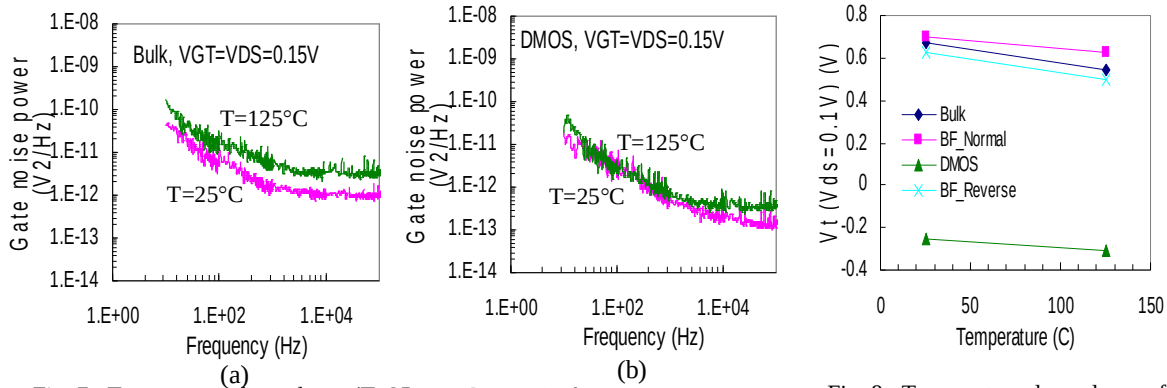


Fig. 7. Temperature dependence (T=25°C and 125°C) of gate noise power in (a) Bulk (b) DMOS

Fig. 8. Temperature dependence of Vt of different devices.