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Ultra-Narrow Silicon Nanowire (~ 3 nm) Gate-All-Around MOSFETs

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1. INTRODUCTION

For continuing the transistor scaling, both innovative device structures and new material are needed. Several alternative non-planar multi-gate FET architectures are being explored [1, 2] and among them, the gate-all-around (GAA) FET provides the best possible electrostatic control on the channel potential [3, 4]. Furthermore, the effectiveness of the gate control increases with reduction in channel width and thickness and therefore, GAA nanowire MOSFET structure could be one of the foremost candidates for extreme CMOS scaling.

In this work, we present n- and p-type GAA MOSFETs fabricated on SOI with silicon nanowire (SiNW) of diameter ~ 3 nm as the channel body. We used 4 nm uniformly grown SiO_2 as the gate dielectric and reduced gate overlap – by tight control on gate CD and alignment – onto the source/drain to minimize the parasitic capacitance. The fabricated GAA nanowire transistors show extremely high drive current, near ideal sub-threshold slope (S.S.), low drain-induced barrier lowering (DIBL) and high I_{ON}/I_{OFF} ratio. The device-to device threshold voltage (V_{th}) fluctuations are also low; +/- 0.1V, which indirectly indicate that fabricated nanowires are quite uniform.

2. FABRICATION

Our fabrication process flow is shown in Fig. 1. 200mm (100) SOI wafers with top Si (p-type, ~10^{15}/cm^3) of thickness 200 nm on 150 nm thick buried oxide (BOX) were used as starting material. Active areas were patterned and etched down to the BOX to make ~ 40 nm wide Si-fins of different length between wider source and drain using alt PSM lithography in a KrF scanner followed by dry etch. The patterned Si was then oxidized in dry O_2 at 875˚C for 4.0 hrs which, due to stress limited oxidation results in two Si-cores (nanowires) [6] – one at bottom and other at top of the Si fin. The top nanowire was etched out using dry etching and bottom was released from oxide using wet etch process – 7 min dip in 1:25 DHF. The nanowire release was followed by 4 nm gate oxide growth and 130 nm amorphous silicon (α-Si) deposition. Fig 2(a) shows the tilted view SEM image of SiNW after gate oxide growth. The α-Si deposition was followed by gate patterning and etching. The gate definition is shown in Fig. 2(b). S/D and α-Si gate were then implanted using As/4×10^{15}cm^{-2}/30KeV and BF_2/4×10^{15}cm^{-2}/35KeV for n- and p-MOS respectively. A long S/D activation anneal (950ºC/15min) was used to ensure dopant diffusion uniformly in the gate α-Si and thick nanowire extension regions beneath the gate – reducing the effective channel length. It was followed by the standard metal contact formation and sintering processes. Fig. 3 shows the TEM cross-section of ~ 3 nm diameter SiNW surrounded by a 4 nm thick uniform gate oxide and poly-Si gate.

3. RESULTS AND DISCISSION

Fig. 4 shows the I_d-V_d plot of 350 nm gate length nanowire GAA n- and p-MOSFETs fabricated on 200 nm long SiNWs of diameter ~ 3 nm. The channel structure of the fabricated devices is little complex as it contains the thicker curved extension regions caused by the corner rounding in lithography on both sides of the nanowire as shown in Fig. 2(a). The on-state current (I_{on}) of ~ 6 and ~3 μA are obtained for n- and p-MOS respectively at an operating voltage of 1.2 V ($|V_{gs} - V_{th}|$ = 0.95V and $|V_{ds}|$ = 1.2V). Although not normalized in the figure due to conflict on normalization parameter (diameter or perimeter), the currents when normalized to diameter of the wire – usually the case in literature – are very high (2 mA/μm for NMOS and 1.0 mA/μm for PMOS). In view of 350 nm gate length, the reported drive currents are high and are more than the earlier reports on nanowire transistors [7-10].

Fig. 5 shows the I_d-V_g plot for the same devices. Despite of single implant source/drain with furnace annealing process, the NMOS exhibits near ideal S.S. ~ 66 mV/dec and very low DIBL ~13 mV/V. The p-FET also shows reasonably good S.S. ~84 mV/dec and DIBL ~34 mV/V. The off-state currents (I_{off}) are in pico ampere regime with I_{on}/I_{off} ratio > 10^6. It may be interesting to mention that almost similar gate control was reported with 9 nm deposited oxide as the gate dielectric on 5 nm diameter nanowire GAA FETs [5]. This indicates a major advantage of GAA nanowire devices as the oxide scaling becomes one of the limiting-factors for conventional MOSFET device structures.

As described above, the gate control on the channel potential is very good in GAA nanowire devices. However, we notice that the threshold voltages are asymmetric ($|V_{thn}|>|V_{thp}|$) (Fig. 5). This asymmetry is due to the fact that the starting silicon is p-type and no channel implants are used in the whole fabrication process. As the nanowire could have remained lightly doped p- type, the PMOS devices are found to be "normally on" with a positive threshold (~0.15V). NMOS threshold voltage is found to be 0.22V without the use of any threshold adjust implant.

As expected due to minor fluctuations in the nanowire diameter, we observe nearly ±0.1V variation in the threshold voltages for both the NMOS and PMOS devices. Similarly, the variation of about ±0.5uA in drive current (normalized to 1000nm gate length) is observed. Fig. 6 depicts the variation of the V_{th} and G_{mmax} for different gate length devices indicating a very good process control.

Fig. 7 shows the effective channel length extraction of the nanowire GAA NMOS using gate-drive method. The effective channel length is found to be about 140 nm longer than the physical gate length, which could be because of the gate voltage dependence of source/drain under-diffusions [11]. We are further analyzing this phenomenon.

4. CONCLUSION

We have presented fully CMOS-compatible fabrication method for ultra-thin nanowire GAA MOSFETs with thin grown oxide as gate dielectric. High drive current and excellent gate control are demonstrated. Unusual phenomenon of effective channel length increase is noticed on the fabricated devices.

References

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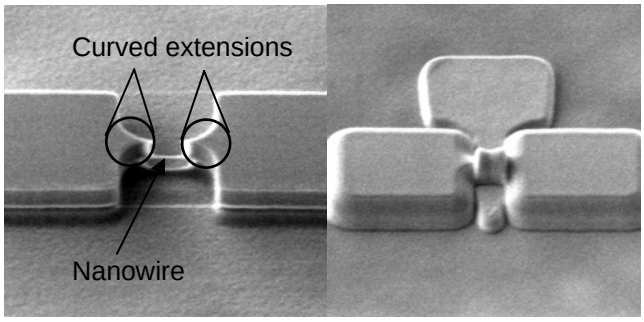
- Fin patterning on SOI and etching of top silicon
- Self limiting oxidation
- Top wire removal using plasma etch
- Nanowire release in DHF
- 4 nm gate oxide growth and 130 nm α-Si dep.
- Gate patterning with minimum overlap
- Gate pattern transfer using plasma etch
- S/D implants: As for NMOS and BF2 for PMOS
- Furnace activation (950° C/15 min)
- Conventional Al metalization and sintering

Fig. 1 Process flow for fabricating SiNW GAA MOS devices



(a) (b)

Fig. 2 Tilted Top view SEM images of: (a) the released 200 nm long nanowire, and (b) after gate electrode definition; 4 nm grown oxide followed by 130 nm amorphous silicon.

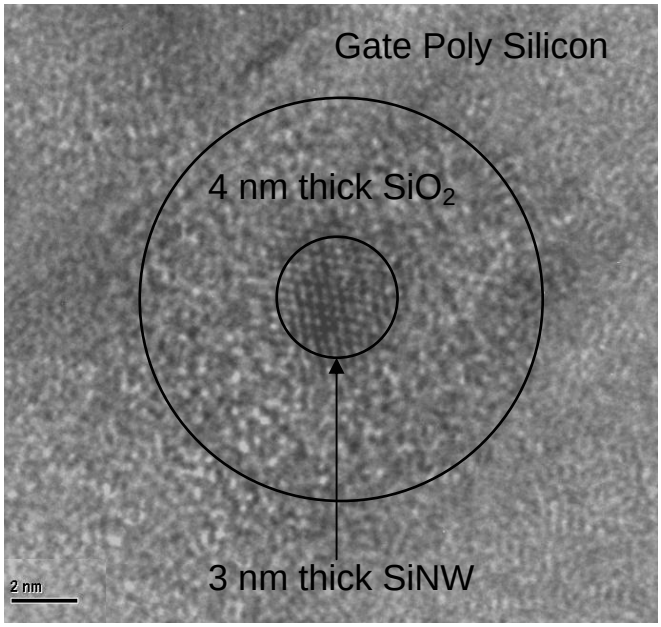


Fig. 3 TEM perpendicular to the nanowire length.

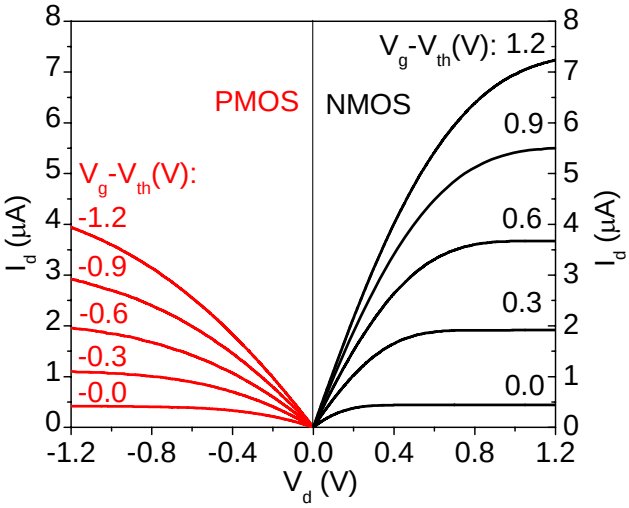


Fig. 4 I_d-V_d plots of GAA SiNW transistors with gate length of 350 nm on a 200 nm long nanowire of diameter 3 nm.

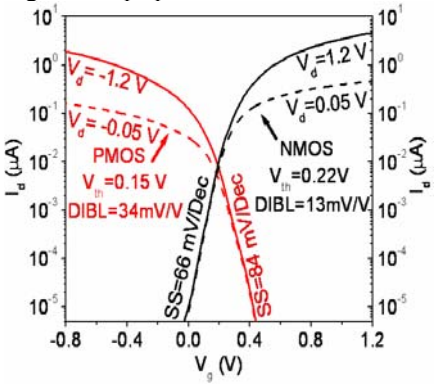


Fig. 5 I_d-V_g plots of GAA SiNW transistors with gate length of 350 nm on a 200 nm long nanowire of diameter 3 nm.

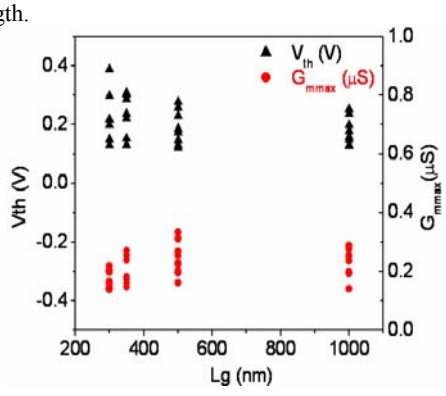


Fig. 6 Threshold voltage and G_{mmax} fluctuations for nanowire NMOS over 10 devices of each gate length (Lg = 300, 350, 500 and 1000 nm). G_{mmax} is normalized to 1000 nm gate length.

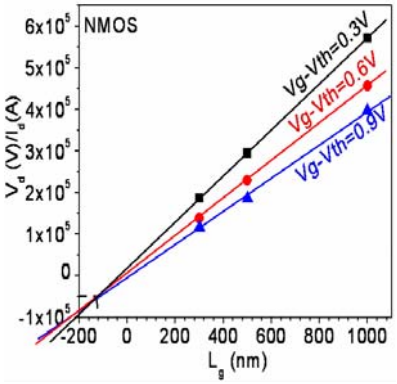


Fig. 7 Effective channel length extraction using gate-drive method. The ratio V_d/I_d is taken at V_d = 45 mV. Three different gate lengths considered are 300, 500 and 1000 nm.