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Local Strained Channel nMOSFETs by Different Poly-Si Gate and SiN Capping Layer Thicknesses: Mobility, Simulation, Size Dependence, and Hot Carrier Stress

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Abstract

13.5% Gm increases as the thickness of SiN capping layer is increased to 250nm. In addition, nMOSFETs with thicker poly-Si layer also exhibit larger Gm. Thicker SiN capping layer didn't necessarily increase the Nit. As to the hot carrier reliability, devices with 170nm SiN capping layer depict well-degradation as compared with other splits with SiN capping layers.

Ⅰ. INTRODUCTION

The local strained channel technique is proposed [1-2]. In this study, we propose a LSC technique that using SiN capping layer deposition with high mechanical stress on single poly-Si gate. In addition, nMOSFETs with thicker poly-Si gate (220 nm) can also increase tensile strain in the channel region compared to that of the thinner (150 nm) poly-Si gate structure. Furthermore, size dependence of nMOSFETs with SiN capping layer is also studied and compared the thickness of SiN and poly-Si gate simultaneously. In the final, reliability of hot carrier injection is studied for all splits[3-5]. The trend of degradation among the splits of SiN capping layer is abnormal to the tensile stress on the channel.

Ⅱ. Device Fabrication

nMOSFETs were fabricated on 6-in wafers. LOCOS is used to isolate the device. Gate dielectric thickness is about 2.2 nm in O_2 ambient. Then, in-situ n-doped poly-Si of thickness from 220, and 150 nm was deposited. Shallow S/D extensions were formed by implanting As (8 keV, $1\times10^{15}cm^{-2}$). After a 200nm TEOS sidewall spacer, deep S/D junctions were formed, and then annealed by RTA at 1000℃ for 10-sec. A LPCVD SiN is deposited on the transistor with different thicknesses from 100 to 250nm. Finally, a four-level metallization was carried out in PVD system for contact.

Ⅲ. Results and Discussion

1. Effects of tensile for devices with W/L=10μm /0.4μm:

Fig. 1 shows the error estimation in V_{TH} versus gate length from 10μm to 0.4μm. The splits with SiN capping layer show worse V_{TH} roll-off as gate length down to 0.4μm. Fig. 2 shows the I_D versus V_D, and the ($Vg-V_{TH}$) is from 0V to 2.0V. A 13.5% increase, as $Vg-V_{TH}$=2.0V, is found as the SiN thickness is 250nm. Fig. 3 shows the Gm versus the splits of different SiN capping layer. It summarizes the strain effects from the thickness of SiN capping layer and poly-Si gate. The tensile stress on the channel mobility is apparent for all splits with SiN capping layer, and about increase 13.5% between the splits of 250nm and without SiN capping layer for both 220nm and 150nm poly-Si gate. In addition, a significant increase about 21% is found form the split of 150nm poly-Si gate without SiN capping layer to that of 220nm poly-Si gate with 250nm SiN capping layer. In addition, the split of 220nm poly-Si gate without SiN capping layer shows larger Gm than that of 150nm poly-Si gate without SiN capping layer. Therefore, thicker poly-Si gate without SiN capping layer also depicts higher tensile stress on the channel.

The simulation stress distribution along the channel of the splits with 250nm SiN layer was depicted in Fig. 4 (a) and (b). For the same SiN capping layer, thicker poly-Si layer would increase the tensile stress along the channel, and then increase the magnitude of mobility. I_{CP} for different SiN capping layers versus V_B is shown in Figs.5 (a) and (b). The ($I_{CP,1M}$- $I_{CP,100K}$) is for the purpose of leakage current correction[6]. For 220nm poly-Si gate splits, as shown in Fig. 5(a), the sequence of I_{CP} is that W/O < 250nm < 100nm < 170nm. It is interesting that thicker SiN layer could lead higher Gm due to higher tensile stress, but not necessarily increase the number of interface trap. This phenomenon could be explained that the precursors for SiN capping layer deposition are SiH_4 and NH_3, a large amount of hydrogen species can be introduced during processing, and then passivate the interface trap. In addition, for 150nm poly-Si gate splits, as shown in Fig. 5(b), the sequence of I_{CP} is that without < 250nm < 170nm < 100nm, which shows different trend from the splits of 220nm poly-Si gate. The I_{CP} begins to decrease due to interface charge passivation.

2. Size dependence for Local Strain n-channel MOSFETs:

Gm for nMOSFETs of different gate length versus different SiN capping layers is measured, as shown in Figs.6 (a) and (b). The devices without SiN capping layer is taken as the control sample. Other nMOSFETs with different SiN capping layers are measured for different device gate length. From Fig.6 (a), it can be seen that the splits of 220nm poly-Si gate with 100nm SiN capping layer for W/L=10μm/1μm depicts mobility un-enhancement behavior. On the other hand, as the gate length attain to 0.6μm for the splits of 150nm poly-Si gate with 100nm SiN capping layer, the Gm is almost the same as the control splits. In addition, as the device size attain to W/L=10μm/10μm, degraded Gm is depicted for all splits.

Several factors, such as tensile stress, increasing number of interface charge, and the ability of interface charge passivation, decide the mobility behavior. Therefore, for short channel nMOSFETs, tensile stress due to local strain dominant the mobility behavior. However, for long channel nMOSFET, the increasing number of interface charge (Nit) due to SiN capping layer degrade the carrier mobility.

3. Hot Carrier Stress of Local Strain nMOSFETs:

Figs. 7 (a) and (b) show V_{TH} degradations. nMOSFETs with SiN capping layer show larger ΔV_{TH} than that W/O SiN capping layer due to impact ionization. In addition, the splits of 250nm SiN capping layer depict the worst V_{TH} degradation. This is because lower bandgap to make impact ionization easier. However, it is noted that the ΔV_{TH} of the splits of 220nm and 150nm poly-Si gate with 170nm SiN capping layer shows the lowest ΔV_{TH} among the devices with SiN capping layers. By comparing Fig. 7(a) with (b), the splits of 250nm poly-Si gate with different SiN capping layer show larger ΔV_{TH} than that of 150nm poly-Si gate. However, there is almost no difference between the splits W/O SiN capping layer.

Figs. 8 (a) and (b) show ΔGm degradation. The splits with 250nm SiN capping layer still depict the worst Gm degradation. The same as V_{TH} degradation, the splits of 170nm SiN capping layer for 220nm and 150nm poly-Si gate is the lowest among the devices with SiN capping layer. Fig. 9 (a) and (b) show the Ig versus Vg. Obviously, the split w/o SiN capping layer depicts the largest substrate injection current among all splits. In addition, the splits with 170nm SiN capping layer, 150n and 220nm poly-Si gate, show the lowest substrate injection current.

In summary, The Gm and current drivability is significantly improved compared to that of the conventional single poly-Si gate device. In addition, the Nit increases as depositing SiN capping layer. However, Nit is not proportional to the thickness of SiN capping layer due to passivate the interface state. Combination of both thick poly-Si gate and SiN capping layer could decrease the device size dependence, and enhance carrier mobility on nMOSFETs. Finally, the splits with SiN capping layer for hot carrier effects depict worse degradation than that without SiN capping layer.

Reference:
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[3] M. Songlp et. al. in IEDM Tech. Dig., 1992, p. 707
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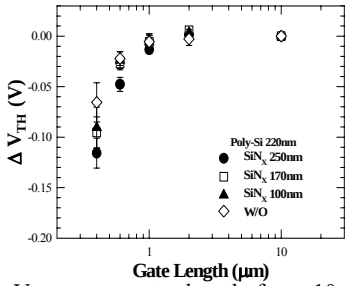

Fig.1 V_{TH} versus gate length from 10μm down to 0.4μm. Every error estimation point is from ten devices 220nm poly-Si gate

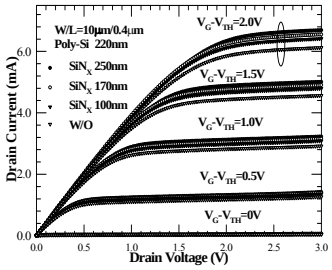

Fig. 2 I_D versus V_D for nMOSFET (W/L=10μm /0.4μm) 220nm poly-Si gate

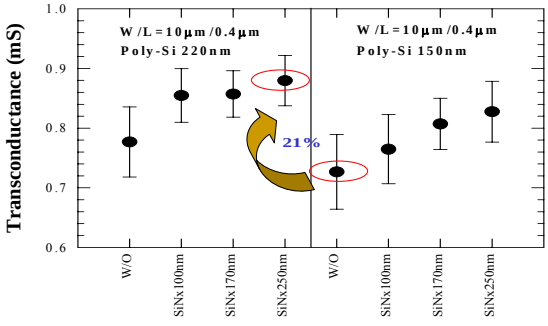

Fig.3 Gm, each point was obtained from 10 devices, versus the splits of different SiN capping layer (W/L=10μm /0.4μm).

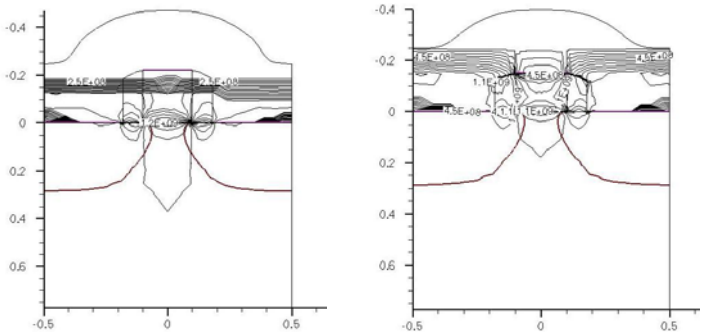

Fig.4 Simulation stress distribution along the channel of the splits with 250nm SiN layer. (a) 220nm (b) 150nm poly-Si gate.

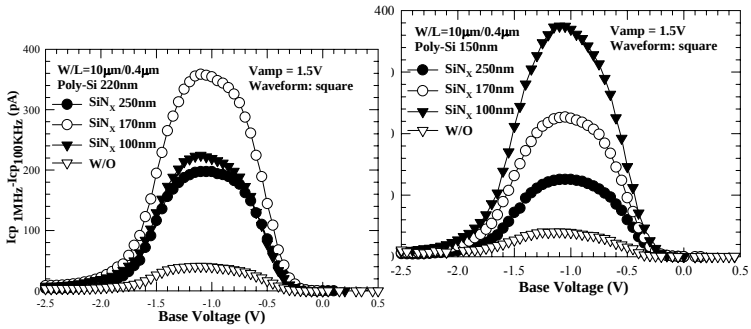

Fig. 5 ($I_{CP,1M}$- $I_{CP,100K}$) of devices for different SiN capping layers versus base voltage (W/L=10μm /0.4μm) (a) 220nm (b) 150nm poly-Si gate. The ($I_{CP,1M}$-$I_{CP,100K}$) is for the purpose of leakage current correction

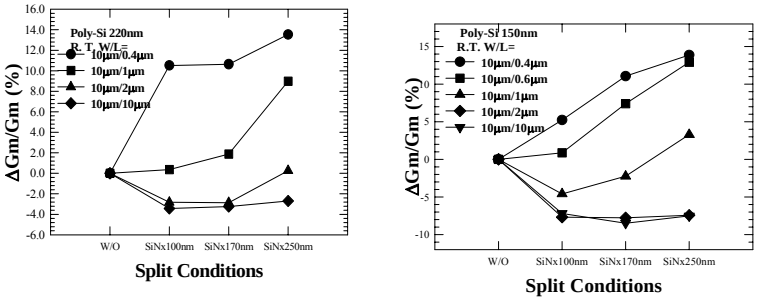

Fig.6 Gm for nMOSFETs of different gate length at room temperature versus different SiN capping layers. (a) 220nm (b) 150nm poly-Si gate. Each point was obtained from 10 devices

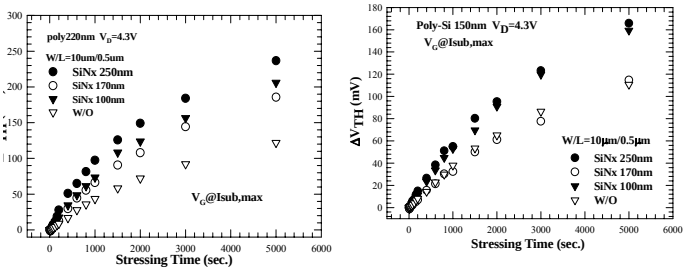

Fig. 7 Stressing time dependence of V_{TH} degradations. Devices are stressed at V_D=4.3V, and V_G is at $I_{SUB,\,max}$ at V_D=4.3V. (a)220nm (b)

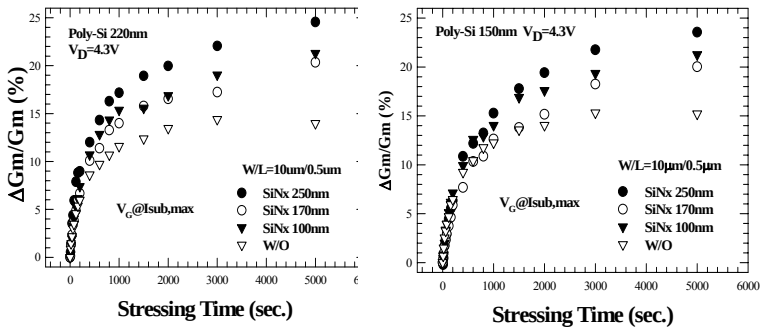

Fig. 8 Stressing time dependence of Gm degradations. Devices are stressed at V_D=4.3V, and V_G is at $I_{SUB,\,max}$ at V_D=4.3V. (a)220nm (b) 150nm poly-Si gate

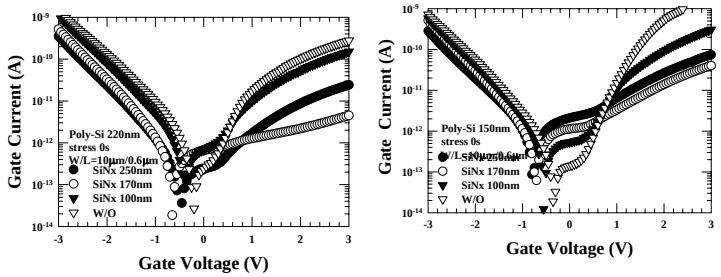

Fig.9 Ig versus gate voltage. the split w/o SiN capping layer depicts the largest substrate injection current among all splits. The splits with 170nm SiN capping layer, 150n and 220nm poly-Si gate, show the lowest substrate injection current. (a) 220nm (b)150nm poly-Si gate