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Characterization of Subthreshold Behavior of Narrow-Channel SOI nMOSFET with Additional Side-Gate Electrodes

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Abstract

An SOI nMOSFET with additional-side-gate electrodes is fabricated and its subthreshold behaviors are discussed. Since the thickness of sidewall oxide equals to that of top one, rather sensitive subthreshold-characteristics control compared with biasing through thick BOX layer is achieved in response to performance requirement.

Introduction

Suppression of stand-by power is one of the key issues on VLSI circuits at present. Therefore, it has been studied to control the threshold voltage of MOSFET by e.g., substrate biasing [1]. For a case of multi-gate devices on SOI, there is some possibility to control device characteristics for respective device independently [2].

From this viewpoint, a narrow-channel SOI MOSFET with additional-side-gate electrodes as shown in Fig. 1 is fabricated and investigated its subthreshold behavior to control its device characteristics. Gate electrode and additional ones on both sidewalls are electrically separated by thermal oxide leading independent biasing to SOI channel. By choosing a thickness of sidewall oxide, rather sensitive subthreshold-characteristics control compared with biasing through thick BOX layer [3] can be expected from a device simulation [4] as shown in Fig. 2.

Device fabrication

A key fabrication process is shown in Fig. 3. P-type, 10 Ω-cm, (100) SOI wafers are used. After formation of SOI narrow-channel of 300 nm in height by RIE and deposition of poly-Si film, subsequent leveling is achieved by CMP. Gate electrode is formed on this surface and covered with its own thermal oxide. Additional side electrodes are delineated by RIE with SiO_2-covered gate as an etching mask. An SEM image for this structure is illustrated in Fig. 4.

Subsequent source and drain formation is achieved by arsenic ion implantation and subsequent rapid thermal annealing. Gate oxide thicknesses are 4.7 nm for top one and 4.8 nm for additional side ones. No channel implantation is performed to evaluate rude channel performance.

Results and Discussion

Since gate electrodes are electrically separated, a few gate biasing modes are available as shown in Fig. 5. I_D-V_D characteristics on these operations of devices with 190 and 480 nm in channel width are shown in Fig. 6. As expected from device simulation, improvements of subthreshold-leakage characteristics by additional biasing, V_{AG} are observed in Fig. 6(a). In addition, threshold-voltage difference between operation modes occurs for both cases.

Figure 7 shows these variations of subthreshold slope and threshold voltage. A subthreshold slope, S is almost 150 mV/decade and threshold-voltage difference from that of tri-gate operation, ΔV_{TH} is small at V_{AG} = -0.5 V. On the other hand, a ΔV_{TH} achieves almost 170 and 171 mV at V_{AG} = -1.0 V, respectively, though these S parameters are held at 95 and 117 mV/decade, respectively.

Detailed dependences of subthreshold-leakage characteristics on V_{AG} are shown in Fig. 8. Leakage currents change sensitively as additional-gate electrodes are biased negative and effectively suppressed for both cases. Figure 9 shows V_{AG} dependence of off-leakage current at some fixed gate voltage. Almost 100-125 mV V_{AG} biasing are needed to achieve a decrease an off-leakage current in one decade.

Conclusion

An SOI nMOSFET with additional-side-gate electrodes is fabricated and discussed its subthreshold behaviors. Threshold-voltage variations and suppression of subthreshold-leakage current are achieved in response to performance requirement by choosing rather small additional-gate biasing. This device structure can provide realistic ciucuit application on the viewpoint of variable threshold-voltage control.

Acknowledgements

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References

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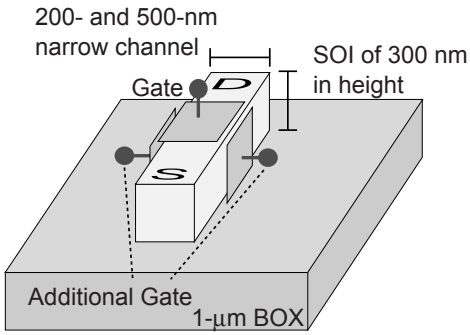

Fig. 1 A narrow-channel SOI MOSFET with additional-gate electrodes. These gates are formed on both sides of an SOI channel.

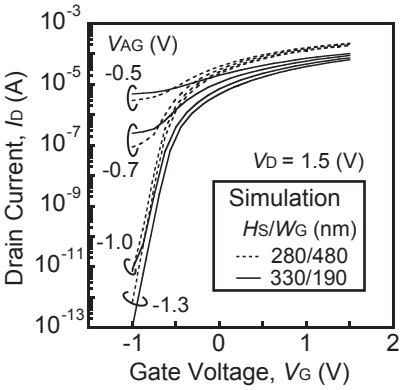

Fig. 2 Simulated I_D-V_G characteristics of the device with gate oxide of 5-nm in thickness. Subthreshold characteristics are improved for both cases as additional-gate are biased negative value.

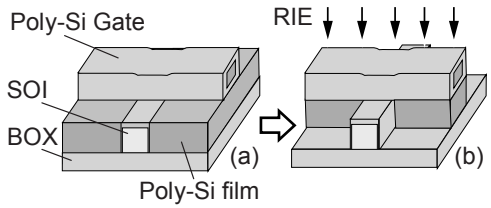

Fig. 3 A key fabrication process of the device. A gate electrode is formed on CMP etch-backed surface (a). Sidewall gates are formed subsequent RIE by using the top gate electrode as an etching mask (b).

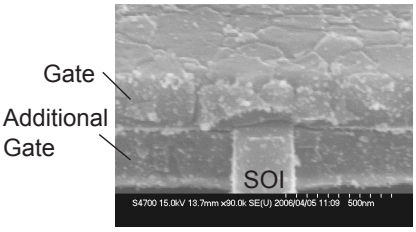

Fig. 4 An SEM image of fabricated structure. Additional-gate electrodes are successfully formed on both side of the narrow SOI channel.

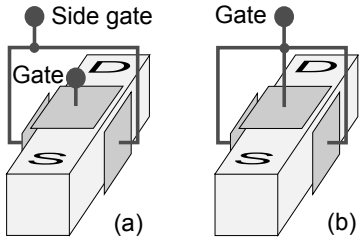

Fig. 5 Gate biasing modes of the device. Fixed side-gate biasing (a) and tri-gate operation (b).

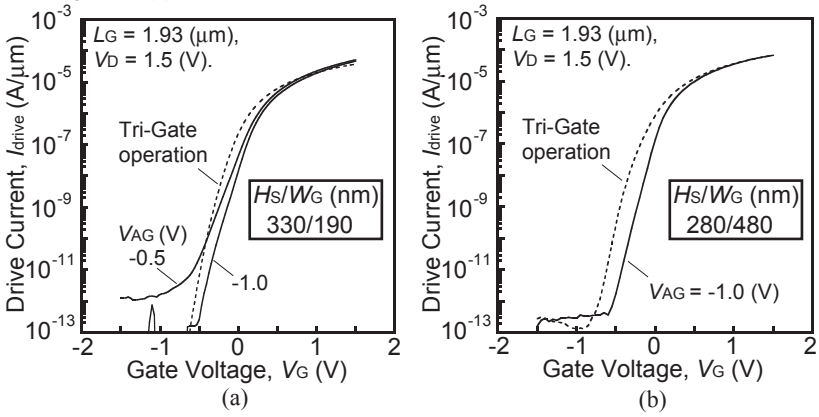

Fig. 6 Experimental I_D-V_G characteristics of the device. Improvement of subthreshold behavior by additional-gate biasing (a) and variation of threshold voltage are observed as expected from a device simulation.

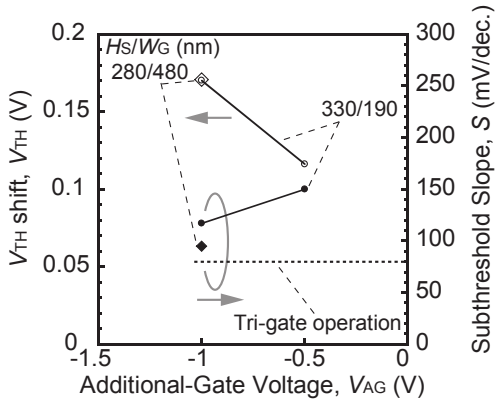

Fig. 7 Dependence of thereshold voltage and subthreshold slope on additional-gate biasing. V_{TH} is defined as gate voltages at drive currents achieve at 100 nA/μm and ΔV_{TH} is V_{TH} difference from that of tri-gate operation.

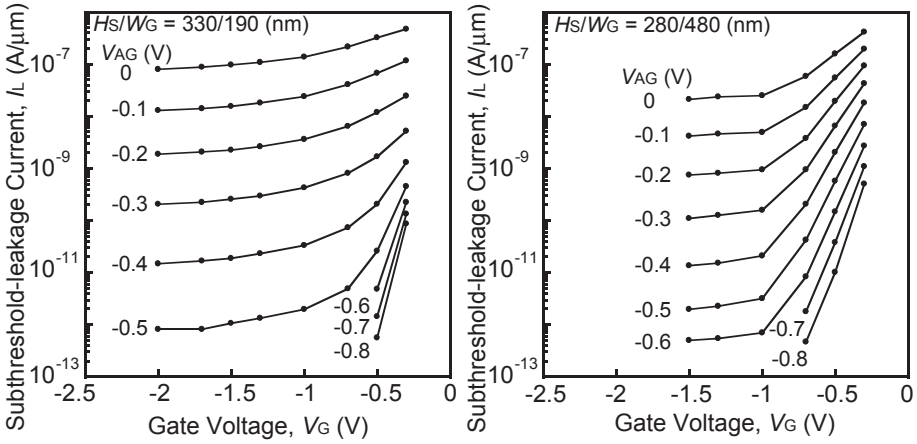

Fig. 8 Detailed subthreshold behavior of the devise. Subthreshold-leakage current changes sensitively as additional-gate are biased negative value and is suppressed effectively for both channel width.

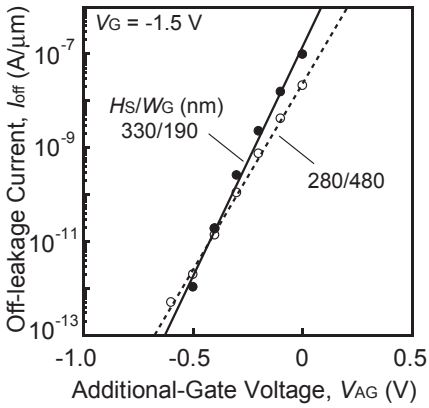

Fig. 9 Off-leakage current characteristics. For decrease in leakage-current, additional gates are need to be biased 101 and 125 mV per decade respectively.