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Gate Capacitance Analysis of Multi-finger MOSFETs for RF Applications

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***Abstract*— In RF CMOS applications MOSFETs with short gate channel length are mainly used, therefore, detailed analysis of the small gate capacitance is needed. A practical gate-to-drain and gate-to-source capacitance model for multi-finger MOSFETs, which consists of small distributed RC circuits and modified BSIM3 based MOSFET models, is developed and verified by $S-parameter$ measurement (frequencies from $2GHz$ to $20GHz$).**

I. INTRODUCTION

Since short gate channel MOSFETs are often used in RF CMOS applications, the gate capacitance value becomes sub-pico Farad. Also, such MOSFETs are fabricated with multi-fingers. A practical model and parameter extraction procedure is needed to characterize these RF MOSFETs. So far, a few papers [1], [2] related to this matter were published, however, these were not focused on multi-finger MOSFETs.

In this research it is shown that 1) development of an RF equivalent circuit model includes the number of MOSFETs, distributed RC silicon substrate, and interconnect parasitic, 2) simple modifications of gate capacitance model at the transition formulation between depletion and inversion regions in BSIM3 version 3.2.4 [3], and 3) RF gate-to-drain and gate-to-source capacitance model parameter extractions and parasitic de-embedding with $S-parameter$ measurements.

II. MODEL DEVELOPMENT

Figure 1 shows the equivalent circuit model of a three terminal RF MOSFET, whose silicon substrate distributed RC and transmission lines are simply represented as lumped-sum modules while keeping the simulation accuracy. Fringing gate-to-drain and gate-to-source capacitance (C_{GDX} andC_{GSX}, respectively) are added externally to the MOSFET array.

The multi-finger MOSFET model consists of the number of modified BSIM3 based MOSFET models. Based on our experimental analysis, drain-to-source voltage (V_{DS}) dependency of gate-to-drain capacitance was not satisfactorily represented in BSIM3. While maintaining the charge conservation we modified the effective gate turn-on voltage for capacitance-voltage calculation (CAPMOD=2, 3) as:

$$V_{GST,effCV} = NOFF \cdot \frac{nkT}{q} \ln\left[1+e^{\left\{\frac{V_{GS,eff}-V_T-V_{DS}(A\cdot V_{DS}+B)}{NOFF\cdot\frac{nkT}{q}}\right\}}\right],$$

here, $NOFF$ is a smoothing parameter in BSIM3, n is the ideal factor, $k$is the Boltzman constant, T is the temperature, V_T is the thermal voltage, $V_{GS,eff}$ is the effective gate voltage. Symbols$A$ and B are newly added to hold V_{DS} dependency, especially in the region from depletion to weak inversion. The modified model was implemented into UCB SPICE3f5 simulator for model verifications.

III. CHARACTERIZATIONS

To verify the model gate capacitance of a 64 gate fingers' MOSFET whose drawn channel length and width of each finger are $0.18\mu m$ and $2.5\mu m$(total channel width is $160\mu m$), respectively, has been measured by converting $S-parameter$ measurement frequencies from $2GHz$ to $20GHz$, whereas capacitance analyzers could not be used in such frequency ranges. As shown in figure 2, 3, 4, and 5, both of gate-to-drain and gate-to-source capacitance are shown good agreement between measurements and simulations, which certify both gate-to-source and drain-to-source bias dependencies of our model. Since unity gain frequency, f_t strongly depends on C_{GS} and C_{GD}, figure 6 can be a good indicator to verify our model equation accuracy. Also, figure 7 can be an indicator to evaluate our parasitic components circuit model because maximum oscillation frequency f_{max} is depends also on parasitic resistance.

IV. CONCLUSIONS

A practical gate capacitance model of RF multi-finger MOSFETs has been developed and verified by measurements and parameter extractions. Using the model RF CMOS performance was analyzed with RF design parameters, f_t and f_{max}. The results and the procedure are useful for RF CMOS circuit designers.

V. REFERENCES

1) J. Dobes, "Smoothing Gate Capacitance Models for CMOS Radio Frequency and Microwave Integrated Circuits CAD," IEEE MTTS Digest, IF-TU-59, pp. 605-608, 2002.
2) H. Aoki and M. Shimasue, "Leaky Large Area Gate Capacitance Extraction for Nanometer CMOS Technology Used for RF Applications," IMFEDK 2004, July 2004.
3) W. Liu, et..al, "BSIM3v3.2.2 MOSFET Model Users Manual, " UCB, 1999.

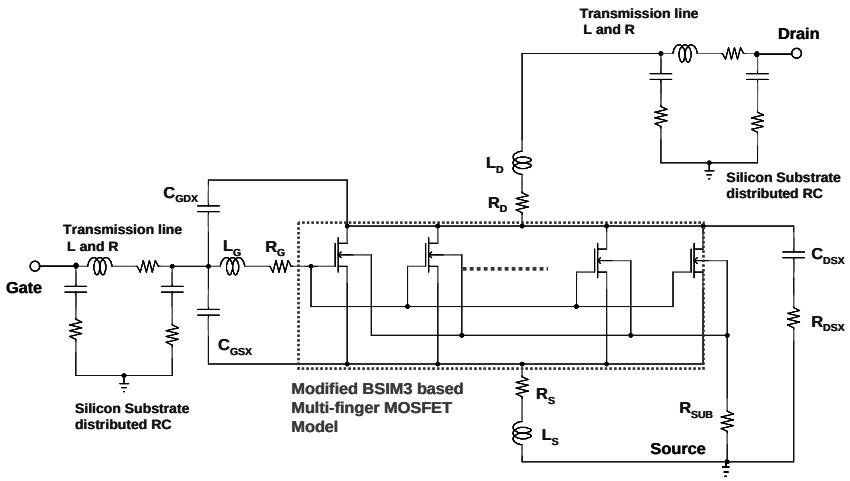

Fig. 1 Equivalent circuit of three terminal RF MOSFET model. The intrinsic part, which is surrounded by a broken box, includes 64 MOSFETs that are the number of gate fingers.

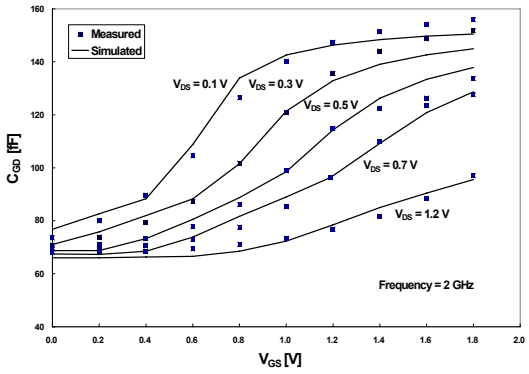

Fig. 2 V_{GS} dependencies of gate-to-drain capacitance*.

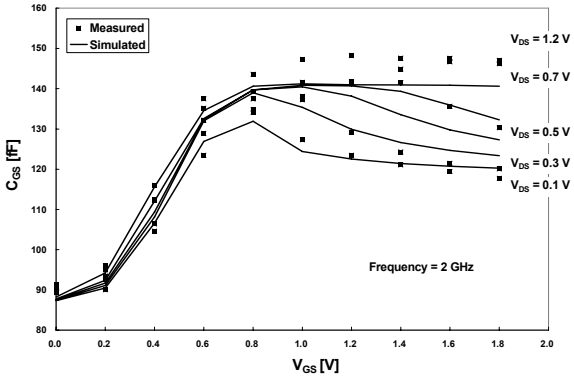

Fig. 3 V_{GS} dependencies of gate-to-source capacitance*.

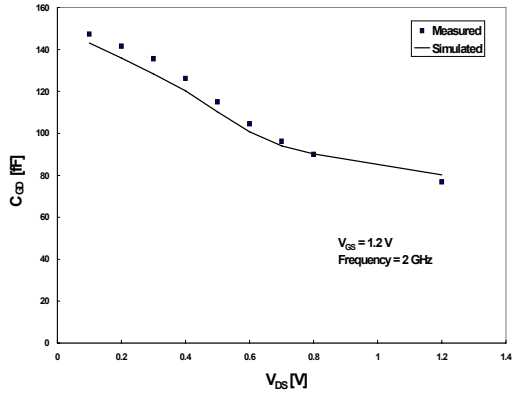

Fig. 4 V_{DS} dependency of gate-to-drain capacitance*.

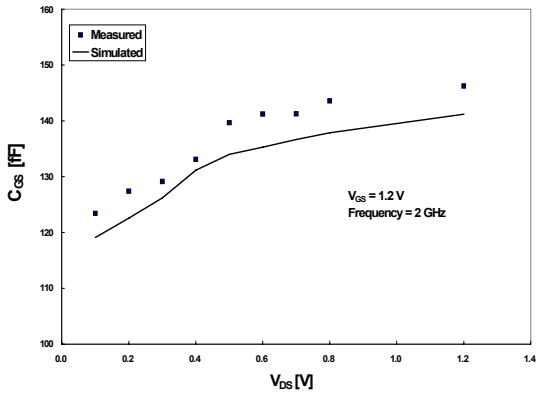

Fig. 5 V_{DS} dependency of gate-to-source capacitance*.

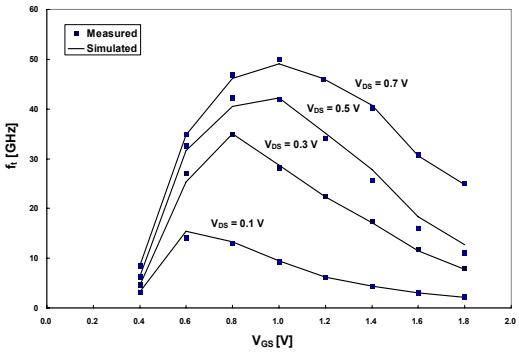

Fig. 6 Unity gain frequency (f_t) characteristics of V_{GS} and V_{DS}*.

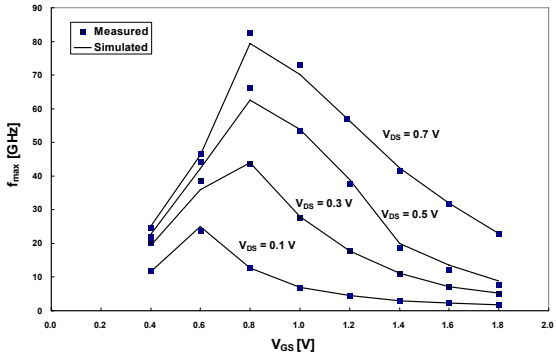

Fig. 7 Maximum oscillation Frequency (f_{max}) characteristics of V_{GS} and V_{DS}*.

* In this experiment a 64 gate fingers' MOSFET whose gate thin-film thickness is *4.0nm* are used. The measured capacitance is de-embedded and converted from *S-parameters* that are obtained by a two-port network analyzer.