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Characteristics of Poly-Si Nanowire Thin Film Transistors with Double-Gated Structures

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1. Introduction

Poly-Si thin-film transistors (TFTs) are widely used in a variety of applications, especially liquid crystal displays (LCDs). However, the performance of conventional poly-Si TFTs is far from satisfactory in terms of speed and current drive [1]. It has been experimentally demonstrated that double-gated TFTs can provide a higher ON current, reduced short channel effects, and a steeper subthreshold slope (S.S.) [2], [3]. While double-gated structure is attractive, the fabrication of high-performance double-gated device is difficult. On the other hand, TFT with nanowire (NW) channel is an alternative approach to improve device properties [4]. Due to its small volume, fewer defects and grain boundaries exist in poly-Si NWs, leading to lower leakage current, higher carrier mobility and better S.S. Also owing to the tiny body of NW, gate can exhibit stronger control over the channel resulting in improved short channel effects [4]. Recently, the present authors have proposed a novel technique to fabricate poly-Si NW TFTs via a very simple process flow [5]. In this work, a unique double-gated scheme that could be constructed in a simple and straightforward manner is proposed. As shown in Fig. 1, the sub-gate and main-gate are aligned just above and abutting the channel, respectively. We have successfully demonstrated and characterized double-gated TFTs with NW channels. Tunable threshold voltage (V_{th}) of NW channels adjusted by the sub-gate will also be discussed.

2. Device Fabrication

The devices were fabricated with a similar process sequence as that described in the previous work [5]. The schematic illustration of the structure is shown in Fig. 1. The major feature is that the two NW channels are formed on the sidewall of the main-gate. The gate oxide was a 40nm-thick TEOS deposited by LPCVD. Furthermore, source and drain (S/D) regions were defined simultaneously with the formation of NW channels in a self-aligned manner. After depositing a 2000 Å TEOS passivation layer, a 5000 Å Al layer was then deposited and patterned to serve as the sub-gate electrode. Note that the passivation layer also served as the sub-gate oxide. The fabricated devices received NH_3 plasma treatment for 3 hours for performance improvement

3. Results and Discussion

The devices can be operated either in single-gated (SG) or double-gated (DG) mode. In SG mode, the sub-gate electrode is grounded, whereas in DG mode, the main gate and sub-gate electrode are connected together to serve as the control gate. Fig. 2 shows the transfer and output characteristics for operations in SG and DG modes. It is clear to see that the performance is enhanced in terms of larger ON/OFF current ratio and better S.S. under DG mode of operation. The field-effect mobility (extracted at V_G = 0.5 V) increases from 50 cm^2/V-s (SG mode) to 61 cm^2/V-s (DG mode). From Fig. 2(b), at $V_D = V_G$ = 5 V, the I_D of DG mode is 1.4 times that of SG mode. These improvements are mainly ascribed to a stronger gate control under DG mode

In addition to DG operation, the independently applied sub-gate bias can also be used to tune V_{th} of NW channels. Fig. 3(a) shows the I_D-V_G curves by varying the sub-gate voltage (V_{sub}) from 4 V to -4 V. In the OFF region, all the I_{OFF} at different V_{sub} coincide with each other, indicating that the leakage mechanism is not dependent on the sub-gate bias. However, I_{min} becomes higher with more positive V_{sub}, due probably to the weak inversion at positive V_{sub} and the strong depletion at negative V_{sub}. To examine this phenomenon, all curves were re-plotted by subtracting the I_{OFF} of V_{sub} = -4 V, as shown in Fig. 3(b). The result reveals that all the curves have essentially the same I_{min}. On the other hand, it is also found that the V_{th} is linearly modulated with the applied sub-gate bias, as depicted in Fig. 4(a). And the amount of V_{th} shift per unit range of V_{sub} is dependent on the channel length. Fig. 4(b) illustrates the dependence of the average ΔV_{th} (from V_{sub} = -4 V to 4 V) on the channel length. In short, V_{th} could be tuned to a suitable range in a reliable manner.

4. Conclusion

A novel NW TFT configured with a double-gate structure is fabricated using simple processing. The device operated in DG mode has been demonstrated with better device performance, including larger ON/OFF current ratio, steeper S.S. and higher carrier mobility. Furthermore, the V_{th} can be tuned by adjusting the sub-gate bias. The amount of V_{th} shift modulated by sub-gate depends on the channel length.

Acknowledgments

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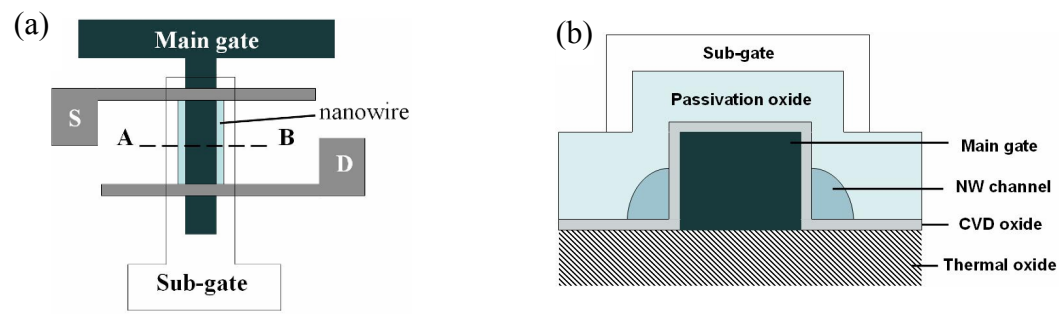

Fig. 1 (a) Top view of the NW TFT with double-gated structure, (b) cross-sectional view of the device along A-B in (a).

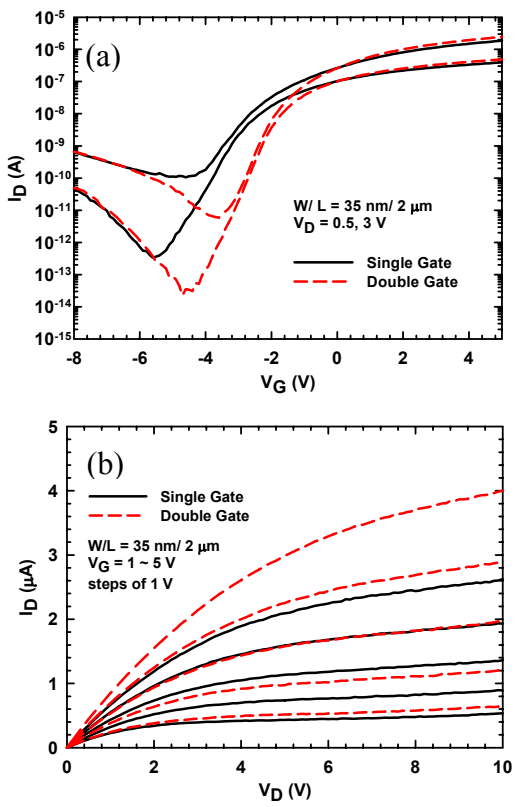

Fig. 2 (a) Transfer and (b) output characteristics of the NW TFT under single- and double-gated operations.

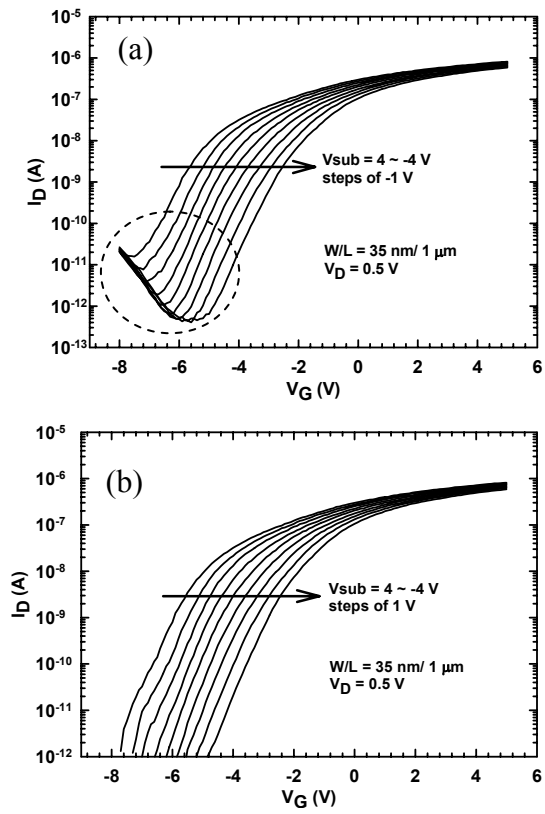

Fig. 3 (a) I_D-V_G characteristics with various sub-gate biases, (b) the modified curves obtained by subtracting I_{OFF} @ V_{sub} = -4 V.

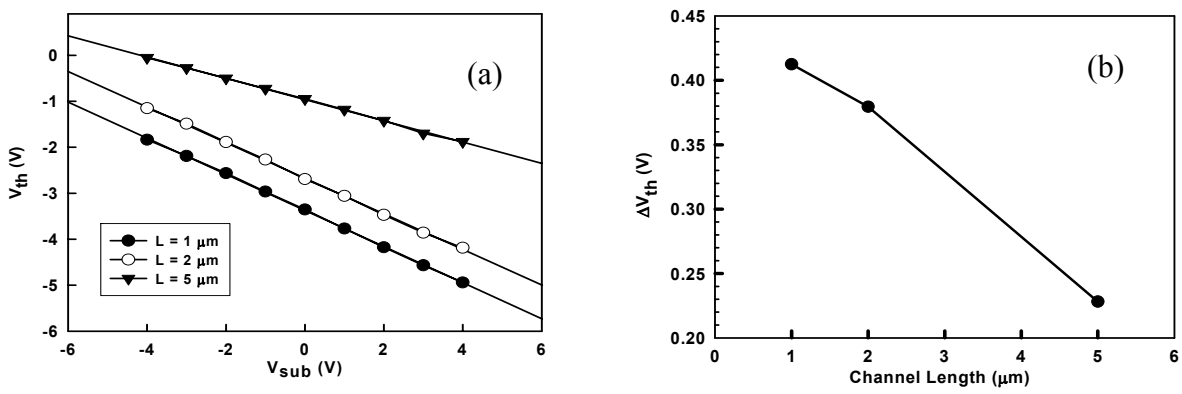

Fig. 4 (a) V_{th} modulation with V_{sub} varying from 4 to -4 V with steps of 1 V for different channel lengths, (b) the dependence of average V_{th} shift per V_{sub} on the channel length.