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Efficient Improvement on Device Performance for sub-90nm CMOSFETs

Chien-Ting Lin[1], Yean-Kuen Fang[1], Chieh-Ming Lai[1], Wen-Kuan Yeh[2], Chia-Wei Hsu[2], Che-Hua Hsu[3], Liang-Wei Chen[3], Mike Ma[3]

1. Institute of Microelectronics, National Cheng Kung University, Taiwan.

2. Department of Electrical Engineering, National University of Kaohsiung, Taiwan.

3. United Microelectronics Corporation, Central R&D Division

No. 1 University Road, Tainan, TAIWAN, 70101, Tel: 886-6-2080398, FAX: +886-6-2345482 e-mail: ykfang@eembox.ee.ncku.edu.tw

1. Introduction

As CMOSFET shrunk to 90-nm node and beyond, issues of low mobility, higher short channel leakages and parasitic capacitances have retarded the device performances. Strained engineering such as a high tensile-stress CESL (Contact Etch Stop Layer) [1] have been extensively implemented to improve device mobility. Notch-gate is a good method to reduce the overlap capacitance between gate to source/drain, and optimize the profile of halo implant to improve the device's SCE [2]; moreover, this higher stress induced by CESL can approach device's channel center, further improving device channel mobility. Therefore, integrating a notch-gate with the stress techniques is an efficient method to obtain high channel mobility, low SCE, and small parasitic capacitance simultaneously. In this work, for the first time, we implemented a high tensile-stress CESL into notch-gate structure. With these technologies, obvious enhancement on CMOSFET performance can be obtained.

2. Device Fabrication

A leading-edge 90nm CMOSFET technology was used as a vehicle to demonstrate device performances. For conventional device (control device), an additional 10nm offset spacer module was implemented. Compared with control device, the notch-gate was produced by adding lateral poly etching on poly bottom, with 10nm lateral notch on each side to form a self-aligned offset spacer. After salicidation, a high tensile-stress CESL (1.1Gpa) was implemented to induce higher channel stress, followed by standard contact and metalization for testing. I-V measurements were performed on probe station using various drain voltages ($|V_D|$=0~1V), gate voltages ($|V_G|$=0~1V). C-V characteristics were carried out with 100kHz from accumulation to inversion region.

3. Results

The schematic view and cross section SEM of the notch-gate devices with tensile stress CESL were shown in Fig. 1 and 2. The V_{th} roll-off characteristic was shown in Fig. 3. For 90nm nMOSFET, because of the optimized halo profile, notch-gate devices possess slight better V_{th} roll-off. Figure 4 shows the I_D-V_D curves for stressed-devices with and without the notch-gate. It found that the notch-gate device possess higher driving capability (~37%) than control devices do. Owing to optimized halo profile [3-4], notch-gate device own higher driving current, lower impurity scattering in the Si/oxide interface and better the SCE. On the other hand, we believed that the extra increase in I_D is presumably due to the CESL-induced tensile stress, which will affect the channel region more directly especially for device's gate was notched. Thus, notch-gate devices possess better device driving capability than control devices do, as shown in Fig. 5. Figure 6 and the insert show the curves of I_D versus V_G-V_{th} in log and linear scale, respectively. For notch-gate device, because more tensile stress was impacted on channel region, generating more interface defects, resulting in slight high subthreshold swing and leakage. Nevertheless in inversion region (inset of Fig. 6), because of the decrease of surface impurity scattering and the apparent impact of tensile stress, notch-gate device with larger channel mobility and higher G_m than control device does , as shown in Fig. 7. Compared with the control device, there is no apparent gate leakage in notch-gate device (Fig. 8). Thus the notch process will not damage the device oxide quality seriously even with the stressed-CESL technique. For notch-gate device, an optimized channel profile with localized halo structure can be found, thus effective junction area between the halo and the source/drain can be reduced, resulting in lower C_j apparently, as shown in Fig. 9(a). Owing to the reduction of the overlap regions from gate to source and drain, the capacitance of gate to source/drain (C_{GD}) is apparent reduced, as shown in Fig. 9(b).

For pMOSFET, the V_{th} versus L_{eff} was shown in Fig. 10. Compared with control devices, notch-gate pMOSFET possesses better V_{th} roll-off. Figure 11 shows the I_D-V_D curves for pMOSFET. The I_D is increased in notch-gate device due to the reduction of channel impurity scattering; however, the increase in pMOSFET is less than in nMOSFET because the tensile CESL-induce stress is inappropriate for pMOSFET [1]. The I_{ON}-I_{OFF} curves for pMOSFET were shown in Fig. 12, the notch-gate devices possess higher mobility than control devices do. But less driving capability improvement is obtained due to the inappropriate tensile stress. The curves of I_D versus V_G-V_{th} in log and linear scale were shown in Fig. 13 and the insert. Similar to the behavior of nMOSFET, slight larger subthreshold swing and leakage current was found in notch-gate pMOSFET due to higher interface defects happen with the impact of tensile stress. Compared with control devices, higher channel mobility and G_m in inversion region can be found in notch-gate device, as shown in Fig. 14. Figure 15 shows the gate oxide leakage of pMOSFET with or without notch-gate. From the gate leakages of nMOSFET (Fig. 8) and pMOSFET (Fig. 15), we believed that the notch-gate technique will not damage the quality of gate oxide apparently. Figure 16 (a) and (b) show the C_j and C_{GD} of pMOSFET, it is apparent that C_j and C_{GD} can be decreased apparently due to the optimized channel profile with localized halo structure and the reduction of the overlap regions from gate to source and drain, respectively.

4. Summary

In this work, we investigated the impact of notch-gate technique on 90nm CMOSFETs with 700A tensile stress CESL. It is obvious that notch-gate structure with the stressed CESL employed will not only suppress the SCE, reduce the C_j and C_{GD}, but also improve the driving capability apparently without increasing the device leakages seriously. Apparent improvement of device driving capability is due to the reduction of surface channel impurity scattering and more direct impact of CESL-induced stress. For pMOSFET, even with inappropriate CESL induced-stress, we found that the notch-gate with optimized channel profile can reduce surface impurity scattering effectively, improving device's driving capability apparently. Therefore, integrating notch-gate structure with a stressed-CESL is a quite efficient method to improve sub-90nm CMOSFET SCE, reduce the parasitic capacitance, and enhance the driving capability simultaneously.

Acknowledgement

The National Science Council of Taiwan, R.O.C., under Contract NSC 94-2215-E-006-005 and 94-2215-E-390-001, supported this work.

References

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[3] D. Wu, *et. al, in Proc. SSIC Tech. Dig.*, 2001, p. 539

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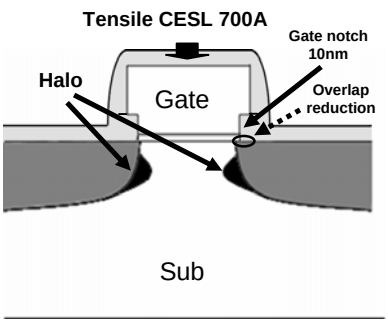

Fig. 1. The schematic view of the notch-gate MOSFET with a tensile CESL.

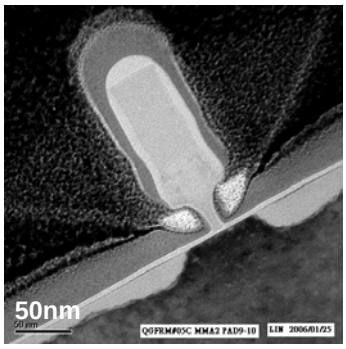

Fig. 2. Cross Section SEM of the notch-gate MOSFET with a tensile CESL.

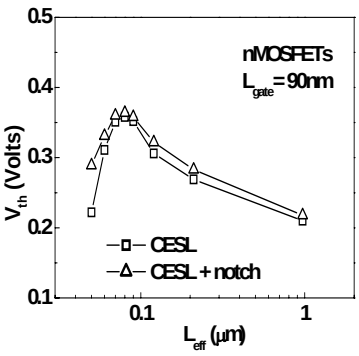

Fig. 3. V_{th} roll-off of CESL nMOSFET with and without notch-gate electrode.

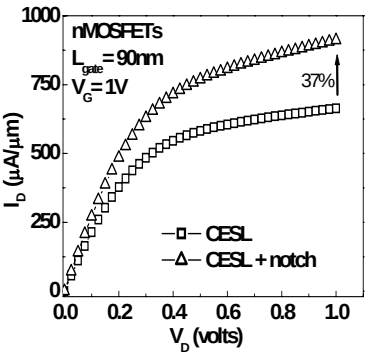

Fig. 4. The I_D-V_D characteristic of CESL nMOSFET with and without notch-gate electrode.

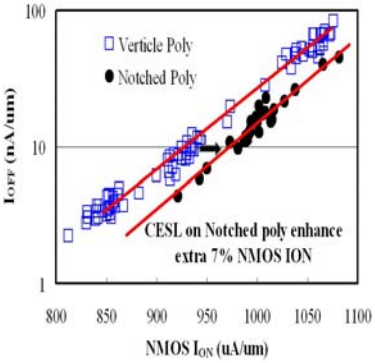

Fig. 5. The I_{ON}-I_{OFF} curves of CESL nMOSFET with and without notch-gate electrode.

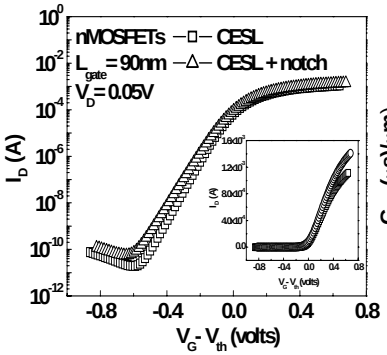

Fig. 6. I_D *vs.* V_G-V_{th} characteristic of CESL nMOSFET with and without notch-gate electrode.

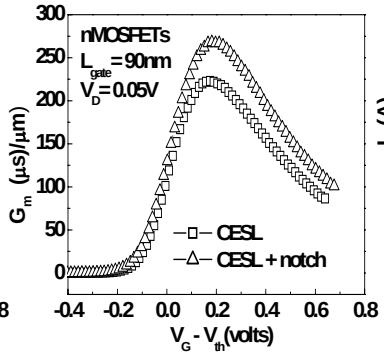

Fig. 7. G_m *vs.* V_G-V_{th} characteristic of CESL nMOSFET with and without notch-gate electrode.

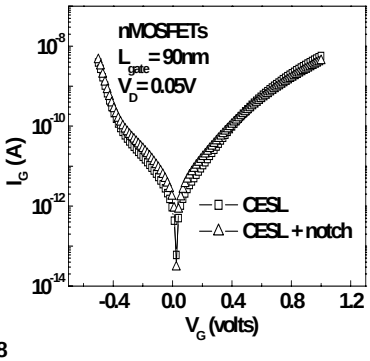

Fig. 8. I_G *vs.* V_G characteristic of CESL nMOSFET with and without notch-gate electrode.

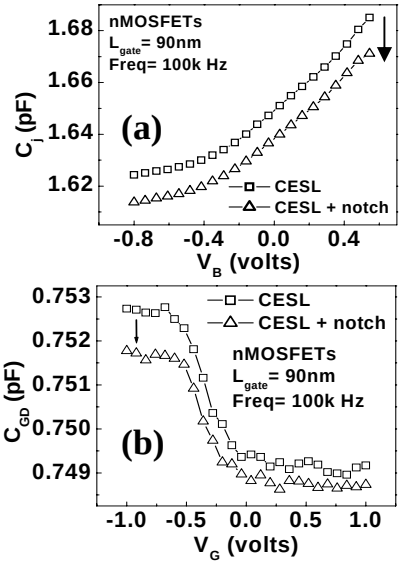

Fig. 9. (a) Junction and (b) overlap capacitances of CESL nMOSFET with and without notch-gate electrode.

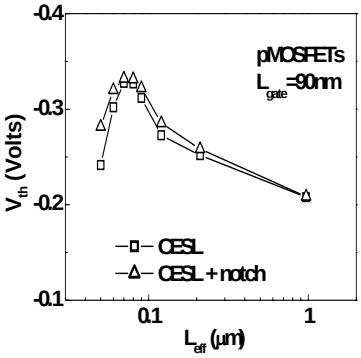

Fig. 10. V_{th} roll-off of CESL pMOSFET with and without notch-gate electrode.

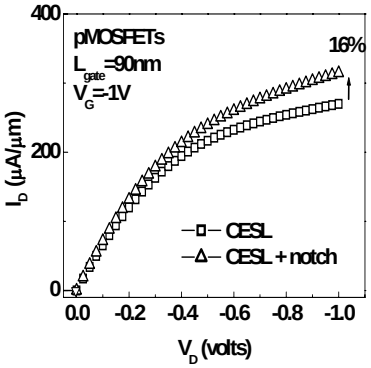

Fig. 11. I_D-V_D characteristic of CESL pMOSFET with and without notch-gate electrode.

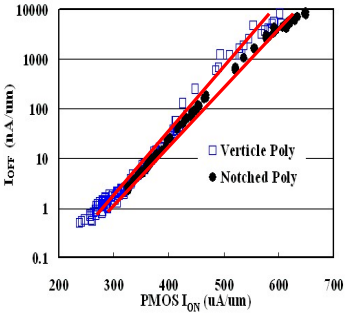

Fig. 12. The I_{ON}-I_{OFF} curves of CESL pMOSFET with and without notch-gate electrode.

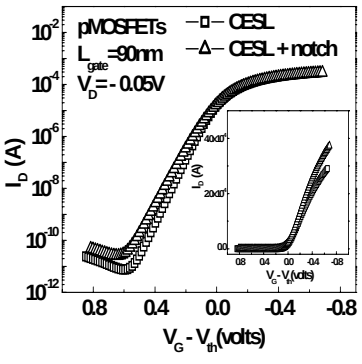

Fig. 13. I_D *vs.* V_G-V_{th} characteristic of CESL pMOSFET with and without notch-gate electrode.

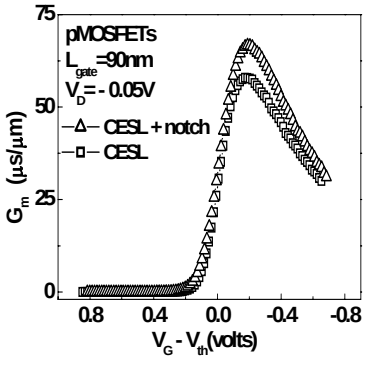

Fig. 14. The G_m *vs.* V_G-V_{th} characteristic of CESL pMOSFET with and without notch-gate electrode.

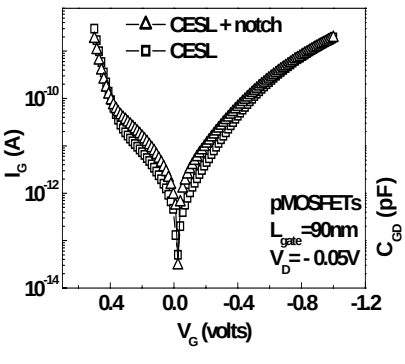

Fig. 15. The I_G *vs.* V_G characteristic of CESL pMOSFET with and without notch-gate electrode.

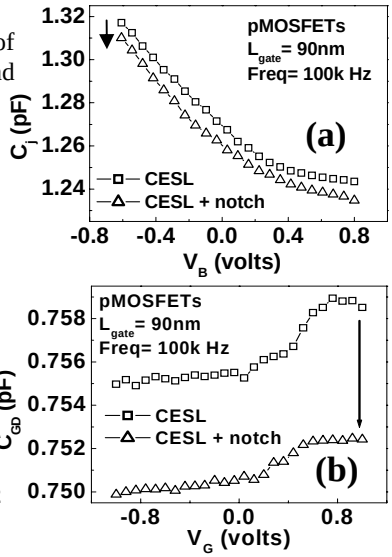

Fig. 16. (a) Junction and (b) overlap capacitances of CESL pMOSFET with and without notch-gate electrode.