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Capacitorless DRAM Cell with Highly Scalable Surrounding Gate Structure

Hoon Jeong, Yeun Seung Lee, Sangwoo Kang, Il Han Park, Woo Young Choi, Hyungcheol Shin, Jong Duk Lee, and Byung-Gook Park

Inter-university Semiconductor Research Center and School of Electrical Engineering, Seoul National University, ENG 420-016, Sillim-dong, Gwank-gu, Seoul, 151-722, Korea
Phone:+82-2-880-7279 Fax: +82-2-882-4658 e-mail: gbhbt@naver.com

1. Introduction

To overcome the scalability issues and process complexity of 1-transistor/1-capacitor DRAM cell, capacitorless 1-transistor (1T) DRAM cells have been recently proposed and investigated [1]. The mainstream 1T DRAM cell is a floating body transistor cell (FBC) which consists of a MOSFET with its body floating electrically. The FBC is implemented by a MOSFET formed on partially depleted silicon-on-insulator (PD-SOI).[2,3] Because the floating body is used as a storage node, the FBC does not require complicated processes for storage capacitor. Therefore, the FBC has a simple process and can be made below $4F^2$. In our previous work, we proposed surrounding gate MOSFET with vertical channel (SGVC cell) as a 1T DRAM cell of FBC type and memory operation was investigated.[4,5]

In this work, we successfully fabricated a highly scalable SGVC cell and the memory effect was investigated for the different body doping concentration.

2. SGVC Cell Operation

Fig. 1 shows the operation principal of SGVC cell. When excess holes are injected in the floating body, the cell state can be regarded as "1" (Body potential increase and V_{th} decrease). On the other hand, when excess holes are swept out of the floating body by forward bias on the body-drain junction, the cell state can be regarded as "0" (V_{th} increase). By measuring the drain current difference between "1" and "0" states of the cell, we can sense whether the majority carriers are accumulated in the floating body. Excess holes can be generated either by impact ionization or by gate induced drain leakage (GIDL).

3. Device Fabrication

Fig. 2 is a 3-dimensional depiction of the SGVC device. A brief introduction to the fabrication process of SGVC cell is given below. It begins with forming the source, channel and drain in the vertical direction on a bulk silicon wafer, by means of controlling the implantation energy. After the division of regions, the pillar type active is made through lithography and trench etching. The gate is created as a sidewall spacer along the pillar type active region. This is how the basic SGVC transistor structure is formed. As can be noted from Fig.2, the top source/drain is connected to the bit line, while the bottom source/drain is shared by all cells. A more detailed process flow chart is given in Fig. 3. The final profile of the fabricated SGVC cell is as shown in the TEM image of Fig. 4. Fig. 5 shows a schematic top-down view of the $4F^2$ 1T DRAM cell. The most prominent advantage of the SGVC cell is that it can have a $4F^2$ structure due to its common source and vertical channel structure, which therefore facilitates the scaling down of the cell array.

4. Experimental Results

Fig. 6 shows I_D-V_D characteristics with various gate voltages. The kink effect is observed. It results from the fact that SGVC cell has a floating body. Fig. 7 shows the device parameter and writing bias of the devices fabricated for comparing the sensing margin with variations in the body doping concentration. The sensing margin of each device was measured at optimum bias conditions by utilizing a transimpedance amplifier.[6] Fig 8. depicts the sensing margin of device 3. The sensing margin was around 6 ㎂ being sufficient enough to be sensed from the current sense amplifier. Also, the read retention time was measured to be about 4 ㎳ which means that the read operation is non-destructive. Fig. 9 shows the sensing margin as a function of body doping concentration. It can be noted that the sensing margin increases when the body doping concentration is decreased. It is a known fact that as the body doping concentration increases the degree of threshold voltage variation with the body potential increases, hence allowing a larger sensing margin. However, in the case of SGVC cells the gate length is determined by the implantation energy and doping concentration, causing the gate length to be shorter when the doping concentration is lower. When the gate length is small, the current level increases and the hole generation through impact ionization increases, subsequently increasing the sensing margin.[7]

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5. Conclusions

We fabricated a new 1T DRAM cell structure (SGVC cell). To compare with conventional 1T DRAM cell, it was integrated on a bulk Si wafer instead of SOI wafer and it can have a $4F^2$ structure due to its common source and vertical source/drain structure. Also, the sensing margin was around 6 ㎂ and read retention time was about 4㎳. It shows the possibility as a 1T DRAM cell. The SGVC cell can be a promising structure for 1T DRAM cell with high scalability and simple process.

References

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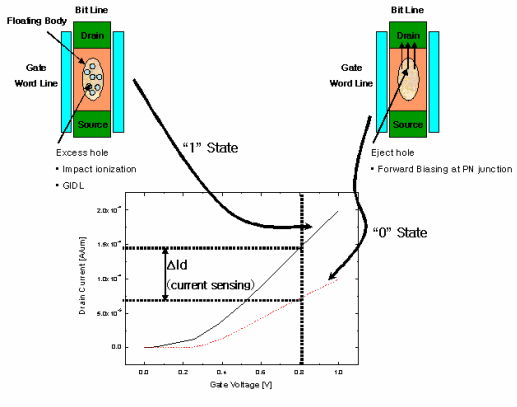

Fig. 1. Principle of surrounding gate 1T-DRAM cell.

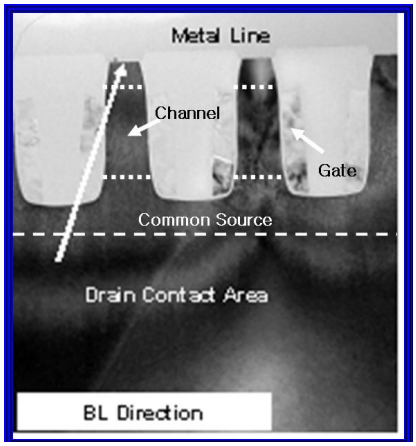

Fig. 4. TEM image of surrounding gate 1T DRAM cell

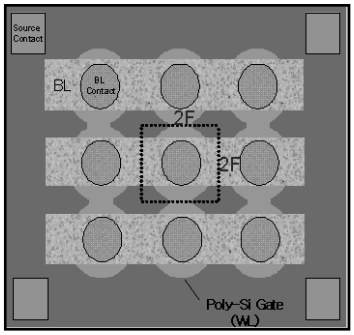

Fig. 5. Schematic top-down view of SGVC cell

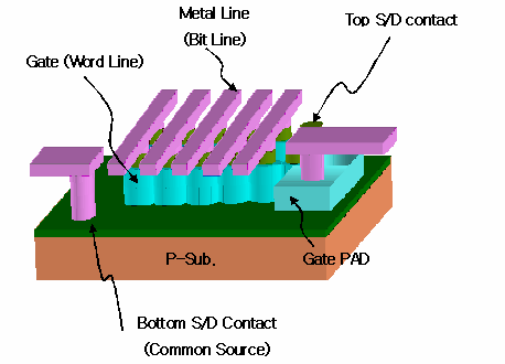

Fig. 2. 3-dimensional depiction of SGVC cell.

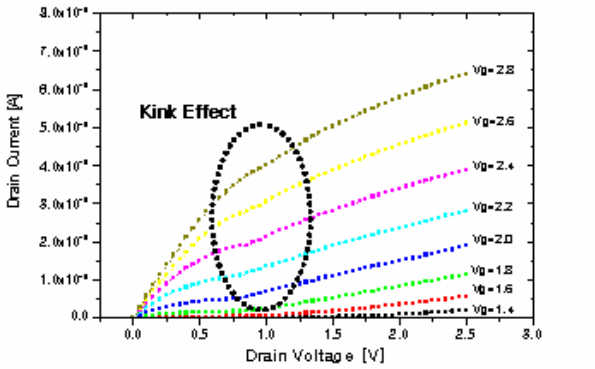

Fig. 6. I_D-V_D characteristics with various gate voltage : The kink effect is observed. It results from the fact that SGVC cell has a floating body

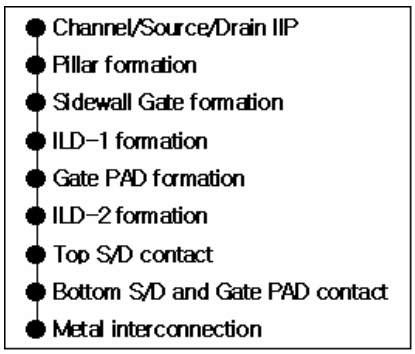

Fig. 3. Process flow of SGVC cell

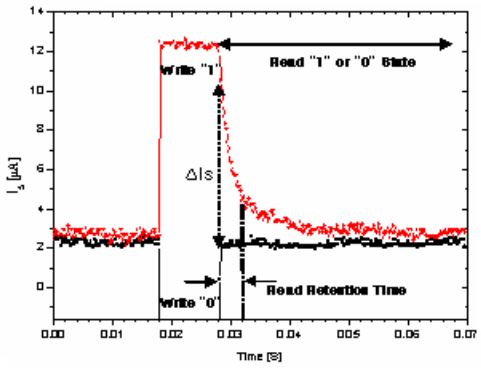

Fig. 7. Measured time dependencies of source current : The difference in source current between the "1" state and "0" state is defined as sensing margin (ΔI_s). Read retention time is defined as the time it takes to reduce sensing margin to 3uA under constant reading condition. The recently developed current sense amplifier is able to detect a current difference down to 3uA.[7]

Device	Voltage	Write "1"	Write "0"	Read
[Device 1] Gate Width (Pillar diameter) = 100 nm Body Doping Concentration = 1×10^{14} [cm^{-3}]	Gate Voltage	3.0 V	3.0 V	3.0 V
	Drain Voltage	2.5 V	-1.2 V	0.1 V
	Source Voltage	0 V	0 V	0 V
[Device 2] Gate Width (Pillar diameter) = 100 nm Body Doping Concentration = 5×10^{13} [cm^{-3}]	Gate Voltage	3.0 V	3.0 V	3.0 V
	Drain Voltage	2.5 V	-1.2 V	0.1 V
	Source Voltage	0 V	0 V	0 V
[Device 3] Gate Width (Pillar diameter) = 100 nm Body Doping Concentration = 9×10^{12} [cm^{-3}]	Gate Voltage	2.0 V	2.0 V	2.0 V
	Drain Voltage	2.5 V	-1.2 V	0.012 V
	Source Voltage	0 V	0 V	0 V

Fig. 8. Device parameters and writing bias

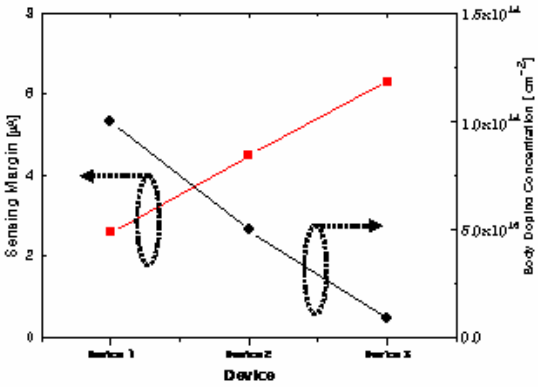

Fig. 9. Sensing margin as a function of body doping concentration