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Cost-Effective and Highly Reliable 6F2 Multi-Gigabit DRAM in 60nm Technology Node for Low Power and High Performance Applications

D. Ha, J.H. Kim, T.H. An, S.S. Lee, S.H. Jang, S.Y. Kim, M.S. Kang, H.T. Kim, S.H. Lee, M.Y. Sim, W.T. Park, D.H. Han, S.M. Jeon, J.W. Park, S.H. Kim, S.H. Kwon, Y.G. Kim, Y.J. Choi, M.S. Sim, C.H. Cho, M.M. Jeong, T.W. Lee, G. Jin, W.S. Lee, and B.-I. Ryu

Advanced Technology Development Team I, Memory Division, Semiconductor Business, Samsung Electronics Co., San#16, Banwol-Dong, Hwasung-City, Gyeonggi-Do, Republic of Korea 445-701
Tel: +82-31-208-2719, Fax: +82-31-209-3274, E-mail: daewon.ha@samsung.com

1. Introduction

Ever increasing memory density requires improved performance and reliability without increasing manufacturing cost and power consumption. In order to satisfy these requirement, several challenges should be overcome; data retention time (T_{REF}), parasitic resistance, process variation, misalignment tolerance, and so on. Cost-effective process integration technologies for multi-gigabit DRAM with robust reliability are presented in this paper.

2. Integration Technology

Table I summarizes the key technologies in this study. Fig.1 shows a cross-sectional SEM image of memory cell array and peripheral circuits. Matured mask fabrication technology and lithography process can achieve sufficient depth-of-focus (DOF > 0.2μm) and reduce CD variation without the need for double-expose-technology [1]. Detail processes can be found in our previous reports [1,2].

Memory Cell Transistor and Capacitor

One of the most critical challenges in 60nm DRAM integration is designing a memory cell transistor without degrading a data retention time (T_{REF}). SRCAT has been adopted in order to increase the L_{EFF}, while maintaining the same physical L_G as RCAT [3] (Fig.2). Negative voltage (V_{SSWL}), applied to word-line during standby period, can reduce the sub-threshold leakage current even for the lower V_T, thus improving T_{REF} due to the reduced junction leakage. Fig.3 shows I_{DS}-V_{GS} characteristics for SRCAT and RCAT, respectively. SRCAT shows better sub-threshold characteristics and lower V_T. GIDL is well suppressed for $|V_{GD}| < 4.5V$ for both SRCAT and RCAT. Reduced number of the channel dopant for SRCAT is very helpful to decrease the statistical V_T variation.

Figs. 4 and 5 show the cross-sectional TEM images and C-V and I-V characteristics for MIM cell capacitor. Laminated high-k dielectrics has a capacitance higher than 25 fF/cell and leakage current less than 0.1 fA/cell. Fig.6 shows the data retention characteristics for SRCAT with and without negative word-line scheme. Optimizing V_{SSWL} and V_T of SRCAT, the excellent T_{REF} is achieved.

Memory Cell Contact

Two critical contacts in memory cell are SAC contact (R_{SAC}) and storage contact (R_{BC}). R_{SAC} between SAC pad and memory cell junction increases exponentially with the contact area which is limited by the physical gate length. Due to large junction leakage, metal contact cannot be directly applied to memory cell junction. Instead, new cleaning process before SAC pad poly-Si deposition has been developed to reduce the contact resistance without aggravating the junction leakage (Fig.7). R_{BC} is dependent on the contact area which is limited by misalignment between storage contact (BC) and SAC pad poly-Si. Fig.8 shows the cross-sectional SEM image of the storage contact. Tungsten storage contact (BC) can significantly reduce the R_{BC} to 1.1kΩ, allowing 20nm misalignment tolerance.

Periphery: Bar-type Contact and Dual Poly-Gate CMOS

For peripheral contacts, it is necessary to increase contact area by replacing the square-type contact with bar-type contact. Enlarged process window for plasma etching was obtained due to small aspect ratio. Fig.9 compares the contact resistance of bit-line on p+ active for square- and bar-type contact. Significantly reduced contact resistance increases the on-current of n/pmos transistors by 6.5/10.5%, and reduces transistor mismatch, especially for sense amplifiers. Fig.10 shows the propagation delay (T_{PD}) of 479 stage unloaded ring oscillator for single poly- and dual poly-gate CMOS. Dual poly-gate CMOS shows a smaller T_{PD} for $V_{DD} < 1.9V$, which is more pronounced for low voltage operation, mainly due to the lower V_T of pmos.

Gate and Capacitor Dielectric Reliability

Fig.11(a) shows TDDB for SRCAT gate dielectric. Although various Si crystal surfaces exist in SRCAT due to its spherical shape, sufficient gate-dielectric-lifetime (> 10 years) can be obtained through optimizing the pre-oxidation cleaning process. Fig.11(b) shows TDDB for MIM cell capacitor with laminated high-k dielectrics.

3. Summary

6F2 multi-gigabit DRAM using 60nm process technology with excellent data retention characteristics, enlarged process window, robust reliability and high performance were successfully demonstrated.

References

[1] C.H. Cho *et al., VLSI Tech*, p.36, 2005.
[2] C.H. Cho *et al., VLSI Tech*, p.32, 2004.
[3] J.Y. Kim *et al., VLSI Tech*, p.34, 2005.

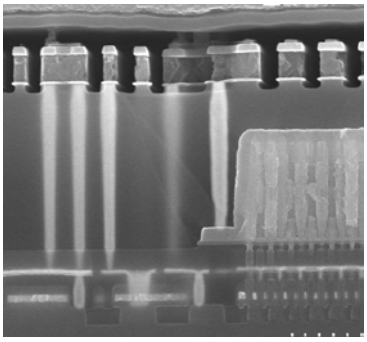

Fig.1 Cross-sectional SEM image of memory cell array and peripheral circuits.

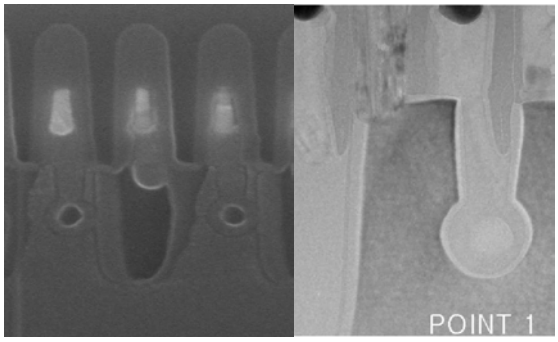

Fig.2 Cross-sectional SEM and TEM images of SRCAT (memory cell transistor), which can increase L_{EFF} while maintaining the same physical L_G.

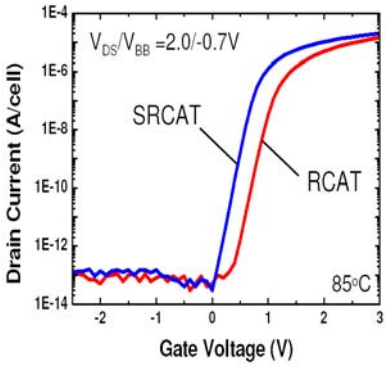

Fig.3 I_{DS}-V_{GS} characteristics SRCAT and RCAT. SRCAT shows better sub-threshold swing and lower V_T.

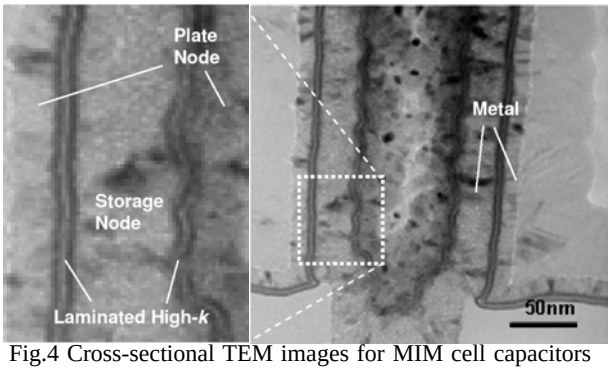

Fig.4 Cross-sectional TEM images for MIM cell capacitors with laminated high-k dielectric.

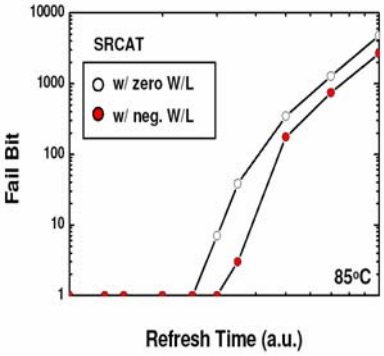

Fig.6 Data retention (T_{REF}) characteristics SRCAT with and without negative word-line scheme. Optimizing V_{SSWL} and V_T can improve T_{REF}.

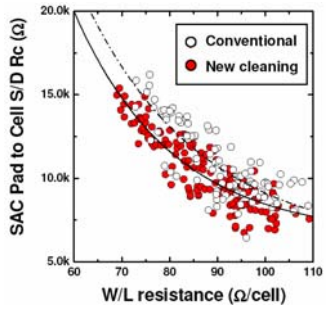

Fig.7 SAC contact resistance (R_{SAC}) is decreased by new cleaning process without aggravating the cell junction leakage current.

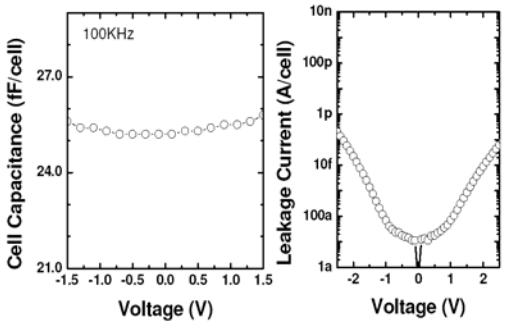

Fig.5 C-V and I-V characteristics for MIM capacitor. Laminated high-k dielectrics has a capacitance higher than 25 fF/cell and leakage current less than 0.1 fA/cell

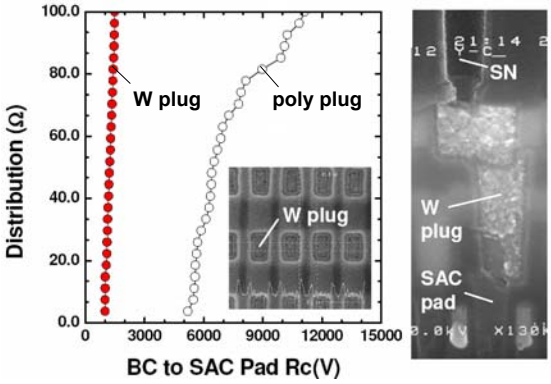

Fig.8 Distribution of storage contact resistance for poly-Si and tungsten plug process. Cross-sectional SEM image of tungsten (W) storage contact.

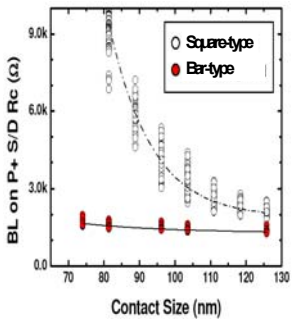

Fig.9 Periphery contact resistance of bit-line on p+ active for square- and bar-type contact.

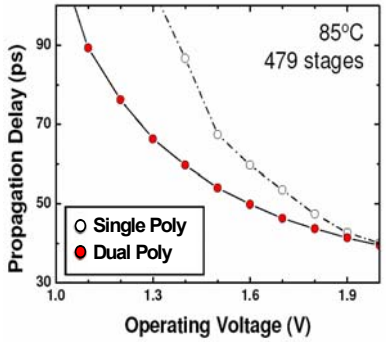

Fig.10 Propagation delay (T_{PD}) of 479 stage unloaded ring oscillator for single poly- and dual poly-gate CMOS. Dual poly-gate shows a smaller T_{PD} for low voltage operation.

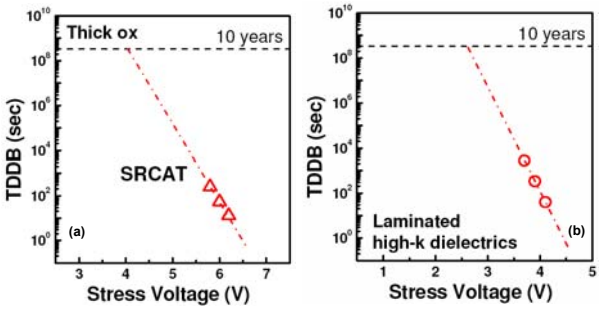

Fig.11 (a) TDDB for SRCAT gate dielectric. Despite of various Si crystal surfaces, sufficient gate dielectric life is achieved. (b) TDDB for laminated high-k dielectric.

Table I. Key process features

Lithography	ArF + mask Tech (OAI/OPC)
Gox	Dual gate oxide (PN SiO_2)
Cell TR	SRCAT + Neg. WL
Peri TR	Dual Poly-Gate Bar-type Contact
STI/ILD	HDP / BPSG
BC	Tungsten plug
Capacitor	MIM structure (laminated high-k)