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Very low voltage operation of p-Si/Al_2O_3/HfO_2/TiO_2/Al_2O_3/Pt single quantum well flash memory devices with good retention

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1. Introduction

Nonvolatile memory devices with a low operation voltage, consuming less power and allowing higher integration with high-speed writing and erasing of data are highly demanded in future scaled memory device applications [1]. A highly scaled polysilicon-oxide-silicon-nitride-oxide-silicon (SONOS) FinFET flash device with poor retention and large operation voltage is reported [2]. Recently, a single (or dual) layer of high-κ charge trapping memory devices or metal nano-crystal memory devices with large operation voltage are also reported by many researchers [3-6]. To meet the ITRS roadmap (operation voltage of memory device <5V), a new HfO_2/TiO_2/Al_2O_3 quantum well memory structure is proposed for the first time. Further improvement of device performance, high-κ Al_2O_3 layers are also used as a blocking oxide and tunneling oxide.

2. Experimental

The starting wafer was p-type Si (100) with resistivity of 15-25 Ω.cm. Prior to deposition of tunneling oxide (Al_2O_3), the p-Si wafers were cleaned by SC1 process. The high-κ Al_2O_3 layer (~5nm) deposited by ALD is used as tunneling oxide. Prior to deposition of TiO_2 layer, a pure HfO_2 film (~2nm) as a wetting layer deposited by ALD system using hafnium tetrachloride ($HfCl_4$) precursor at substrate temperature of 300°C. Then, high-κ TiO_2 film with thickness of ~9nm was deposited by PEALD system using Titanium(IV) Isopropoxide precursor at 350°C. Then, the high-κ Al_2O_3 layer with thickness of ~10nm as a blocking oxide was deposited using trimethylaluminium ($Al(CH_3)_3$) precursor at substrate temperature of 300°C. The post deposition annealing (PDA) treatment at 900°C for 1min in N_2 ambient was performed. Platinum gate (Pt) is used as gate electrode.

For comparison of single quantum well memory capacitor data, a memory transistor of HfO_2(0.5nm)/TiO_2(0.5nm) with 3 quantum wells is fabricated. The tunneling oxide of SiO_2 (~4nm) was grown by RTO system at 1000°C, 1min. The blocking oxide of SiO_2 (~10nm) was deposited by PECVD at 450°C. For simple fabrication process, a poly-Si gate is used for transistor. The post metal annealing with temperature of 400°C and 5 min was done using forming gas ambient for all memory devices.

3. Results and discussion

Fig. 1 shows the high-resolution transmission electron microscope (HRTEM) image of single quantum well memory device after PDA process. It is observed that the HfO_2/TiO_2 film shows fully crystalline while Al_2O_3 film shows almost no crystalline or partial crystalline. It has been shown a clear layer-by-layer structure. Fig. 2 shows x-ray photoelectron spectroscope (XPS) characteristics of HfO_2(0.5nm)/TiO_2(0.5nm) multilayer quantum wells after PDA treatment. It is noted that binding energy of Hf-Ti signals is not changing with pure HfO_2 or pure TiO_2 film after high temperature PDA process, indicating that there is no reaction between Hf and Ti atoms. So, the HfO_2/TiO_2 can be treated as a new material system, which can make a quantum well structure. Valence band maximum of TiO_2 and HfO_2 films is measured by ultraviolet photoelectron spectroscope (UPS) measurement after PDA treatment (not shown here). Assuming the energy band gap of HfO_2 (E_g~5.9eV) and TiO_2 (E_g~3.5eV), the conduction band offsets (ΔE_c) of those films are calculated to be ~1.7 eV for HfO_2 film and ~1.0 eV for TiO_2 film on p-Si substrate. Due to the small conduction band offset (<~1.0eV), more electrons can be injected in the HfO_2/TiO_2/Al_2O_3 quantum well from the Si conduction band. The electron can be stored into the quantum well under small program voltage [Fig. 3(a)]. The stored charges can be easily erased with small negative voltage application because stored charges can come back to the Si conduction layers [Fig. 3(b)]. In this case, a small program/erase voltage is applied on device. A good capacitance-voltage (C-V) hysteresis (C_{ox}>4fF/μm^2) is observed for single quantum well device (Fig. 4). The hysteresis memory window increases with increasing the operation voltage up to 2V. It is also noted that the memory window is going to be saturated at the gate voltage of 2V because of injected carrier saturation in the single quantum well. A maximum memory window of ~1.6V is observed with very small gate voltage operation (V_g=±2V). Note that pure HfO_2 charge trapping layer shows memory window beyond the operation voltage of 5V [6] and pure TiO_2 film does not show any memory window with all operation voltages. It means that the memory window of HfO_2/TiO_2/Al_2O_3 structure is observed due to the carrier confinement in the quantum well. A stretch-out of C-V curve at accumulation region may be due to carrier confinement in the quantum well (Fig. 4). The J-V hysteresis shows the memory window of ~1.5V under the gate voltage of ±2V only (Fig. 5). A negligible leakage current is increased with increasing the measurement temperature (Fig. 6), suggesting that the quantum well structure can be useful in future scaled memory technology with extremely low power operation. It is basically high-κ stack layers deposited by ALD and the memory device has excellent uniformity (Fig. 7). The memory window changes with gate voltage operation, indicating that quantum well flash memory device can be used in multi-bit operation. A negligible charge loss (2% to 5%) is observed up to measurement time of 10^4 seconds (Fig. 8). An excellent retention (memory window of ~1.5V) is observed up to retention time of 10^4 seconds (Fig. 9).

A memory window increases with increasing the number of quantum wells (Fig. 10). A maximum memory window is about 4.2V for HfO_2(0.5nm)/TiO_2(0.5nm) with 3 quantum well memory transistor. So, one quantum well has ~1.4V memory window, suggesting that the memory window can be increased with increasing the number of quantum well and it does not depend on the quantum well thickness. Depending on requirements, the quantum well structure can be designed for scaled memory device applications.

4. Conclusions

Very low voltage operation of HfO_2/TiO_2/Al_2O_3 quantum well structure is proposed. A memory window of ~1.6V is observed under extremely low voltage operation (<2V). The charge loss tends to zero because of carrier confinement in individual quantum well. It is believed that this quantum well flash memory device can be used for mass production.

References

[1] J. D. Lee et al., IEEE EDL, 2002, p. 264 [2] J.-R. Hwang et al., IEDM Tech. Dig., p. 161, 2005 [3] Y. Q. Wang et al., IEDM Tech. Dig., P. 169, 2005. [4] S. Maikap et al., Int'l Symp. on VLSI-TSA, p.36, 2006. [5]Y. J. Ahn et al., Symp. VLSI Tech. Dig., 2006, p. 109. [6] S.Maikap et al., SSDM 2006, accepted.

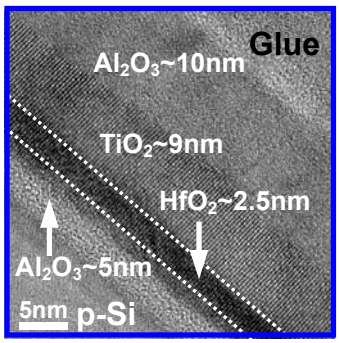

Fig. 1 Cross-sectional high-resolution TEM image of p-Si/Al_2O_3/HfO_2/TiO_2/Al_2O_3/Pt memory structure is shown after 900°C, 1min in N_2 ambient.

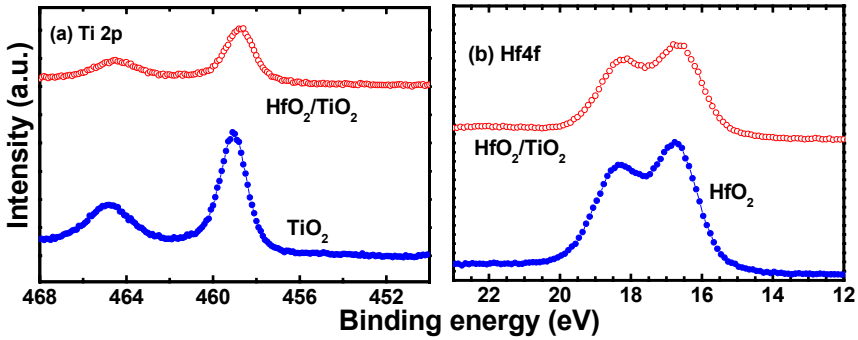

Fig. 2 X-ray photoelectron spectra of (a) Ti 2p and (b) Hf 4f signals for pure TiO_2, pure HfO_2 and HfO_2(0.5nm)/TiO_2(0.5nm) samples after post deposition annealing treatment (900°C, 1min in N_2 ambient).

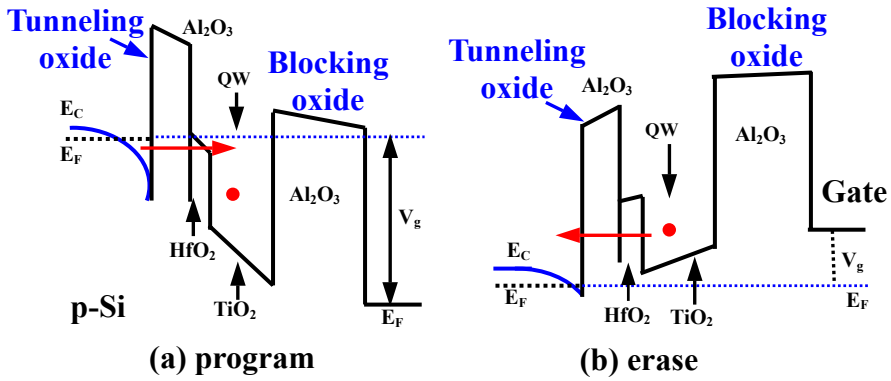

Fig. 3 Schematic energy band diagrams of HfO_2/TiO_2/Al_2O_3 single quantum well (QW) structure with Al_2O_3 as a blocking oxide and tunneling oxide are shown under the devices (a) program mode and (b) erase mode. The high-κ Al_2O_3 as a blocking oxide is used to suppress the backward tunneling current.

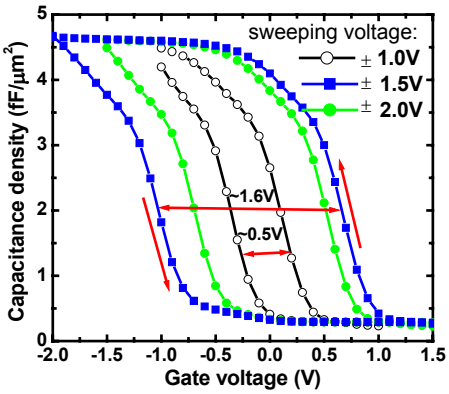

Fig. 4 HFC-V (100kHz) hysteresis of single quantum well memory device. A memory window is observed ~1.6V@ V_g=±2V for single QW device.

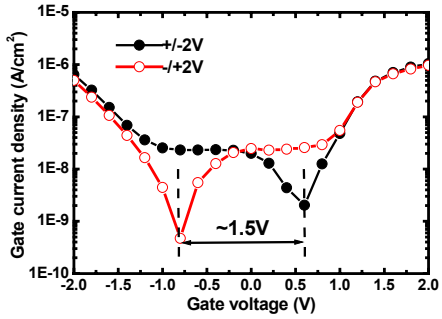

Fig. 5 The current density (J) versus gate voltage (V) hysteresis of single quantum well memory device. A hysteresis memory window of ~1.5V @V_g=±2V is observed.

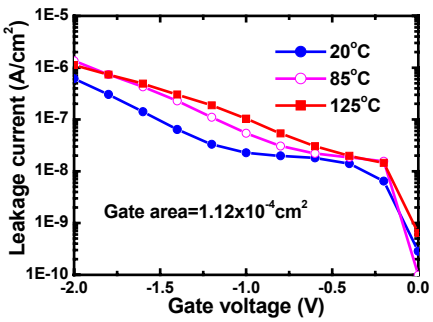

Fig. 6 A negligible leakage current is increased with increasing the measurement temperature.

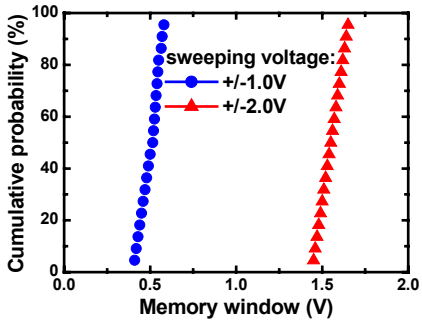

Fig. 7 A good uniformity is observed for quantum well memory devices.

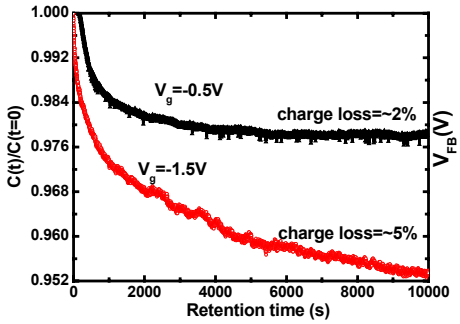

Fig. 8 Discharge characteristics of single quantum well device are plotted. Discharges are studied after V_g =2V, 1s stressed condition.

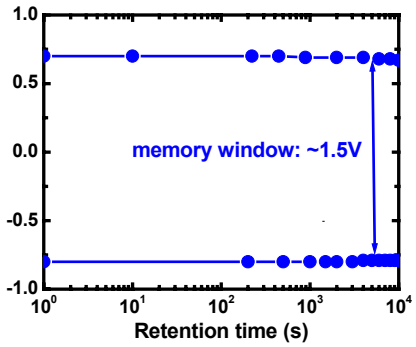

Fig. 9 Retention characteristic of HfO_2/TiO_2/Al_2O_3 single quantum well memory device is plotted.

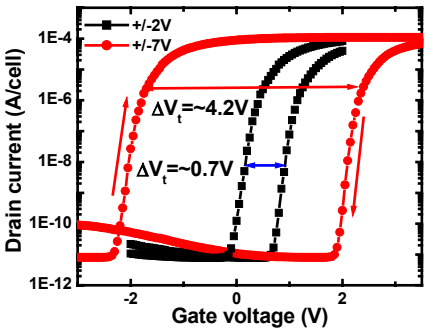

Fig. 10 I_d-V_g hysteresis of memory transistors (WxL=20x20 μm^2) under double sweep measurement.