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FinFET NAND Flash with Nitride/Si Nanocrystal/Nitride Hybrid Trap Layer

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Abstract

The effects of trap layer on NAND Flash performances have been described in this paper. In order to overcome the slower programming speed of the discrete trap memory than conventional floating-gate device, nitride and Si nanocrystal have been assembled together so as to provide the higher trap density for the improved device performance. This hybrid trap layer technology has been applied to the FinFET NAND Flash, and the results show ~5 V of program/erase window with reasonable device reliabilities.

Introduction

As the NAND Flash scaling is accelerated to the device limitation, many researches have been focused to find out the eventual solution for the future Flash structure. Discrete trap memory (DTM), such as SONOS and nanocrystal (NC) memory, is clearly one of the most promising candidates owing to its localized charge storage/loss and floating-gate coupling free structure [1]. However, unlike the conventional floating-gate (FG) device, the program/erase (P/E) window of DTM depends not only on the programming electric field, but on the trap density as well, resulting in the shrinkage of P/E window. Considering that the technological trend of NAND Flash is proceeding toward the MLC operation for the higher bit-density, it is very important to ensure the sufficient P/E window of DTM device.

In this work, trap layer and blocking oxide engineering have been performed to improve the P/E window of DTM device. To improve the erase characteristic such that the electron back tunneling from the control gate can be minimized during the hole injection from the substrate, Al_xO_y is used instead of the conventional blocking oxide [2]. For the enhancement of program characteristic, nitride / Si NC / nitride hybrid trap layer is applied to increase the trap site density. It is believed that Si NC and its transient layer between NC and nitride interface is a major part of the charge trapping in hybrid structure, meaning that it is possible to precisely control the location of the charge storage. Therefore, unlike the conventional SONOS structure where the charge storage is mainly located at the nitride / oxide interface [3], it is possible to obtain the better charge loss reliability by using the hybrid trap layer. All of these technologies are integrated, for the first time, on a FinFET structure for the enhanced scalability of NAND Flash device [4]. The advantages of the FinFET NAND Flash with hybrid trap layer are illustrated in Fig. 1.

Experimental

For the FinFET NAND Flash fabrication with engineered trap layer and blocking oxide, the following processes have been performed. Si fin was formed using the conventional shallow trench isolation (STI) process, including the trimming oxidation and field oxide recess to control the fin width and height, respectively. 3.5 nm-thick SiO_2 were grown by dry oxidation after the active fin formation as a tunnel oxide. For the trap layer, the Si NCs were deposited using a cyclic CVD method with SiH_4 as a seed forming gas at 520~600℃. A top-view SEM of Si NCs on the thin SiN layer (6 nm) is shown in Fig. 2 (c). The mean size of NCs and aerial density turned out to be 7~10 nm and 1×10^{12} cm^{-2}, respectively. For the blocking oxide, the Al_xO_y are deposited by ALD process followed by 1020℃, 30 sec post-deposition anneal. N^+ poly-Si was then deposited and patterned as a gate electrode. Fig. 2 (a) and (b) shows the SEM images of the fabricated NAND string, and well-defined FinFET devices, integrated both on the cell array and GSL/SSL transistors.

Results and Discussion

Fig. 3 shows the I_D-V_G characteristics of the W/L = 63/63 nm FinFETs having 30 nm fin height. I_D-V_G characteristics are measured from WL 0 to WL 31, demonstrating the successful operation of 32 WL NAND string. The I_{DSAT} of the FinFETs are more than 50 % improved compared to the conventional planar device [5], and thus, it is expected to provide the enhanced scalability in terms of the worst-on-cell (WOC) current limitation. To investigate the P/E characteristics of the fabricated device, the threshold voltage shift is measured at WL15 with various pulse amplitude and duration. As shown in Fig. 4 (a), the threshold voltage shift during 20 V, 100 μsec programming reaches up to 5.2 V. The threshold voltage shift during -18 V, 10 msec erasing is about 4 V as shown in Fig. 4 (b). For the comparison, the P/E threshold voltage shifts of the previous Si NC literatures [6,7,8] are plotted in Fig. 5 as a function of the programming electric field. As shown in the figure, both the program and erase characteristics of this work are greatly improved. Considering that the program and erase mechanisms are different in DTM device structure, i.e., electron injection from the substrate during program and hole injection from the substrate during erase, it is believed that the enhanced suppression of the electron injection through the Al_xO_y blocking oxide and the increased number of trap density provided by hybrid trap layer are mainly responsible for the improvement of erase and program characteristics, respectively.

The room temperature charge loss is measured for the investigation of the retention reliability, and the results are shown in Fig. 6. The charge loss can be hardly observed up to 10^4 sec, meaning that the controlling of the trapping location by Si NC is effective. The bake retention characteristic measured after 10K P/E cycles, shown in the inset of Fig. 6, also support this mechanism. Compared to the bake retention result of the device without NC, the hybrid device shows ~15 % improved charge loss and the better uniformity after cycling.

Conclusion

In this work, the engineered trap layer and blocking oxide have been applied to the FinFET structure, and the successful integration of such technology to the NAND Flash device has been demonstrated. The increased trap density of the hybrid trap layer and the enhanced leakage reduction of Al_xO_y are proposed as a dominant mechanism of the larger program and erase window, respectively. The trap location control by NC of hybrid trap layer is proposed as a mean to improve the retention, and the bake retention result was demonstrated to support this mechanism.

References

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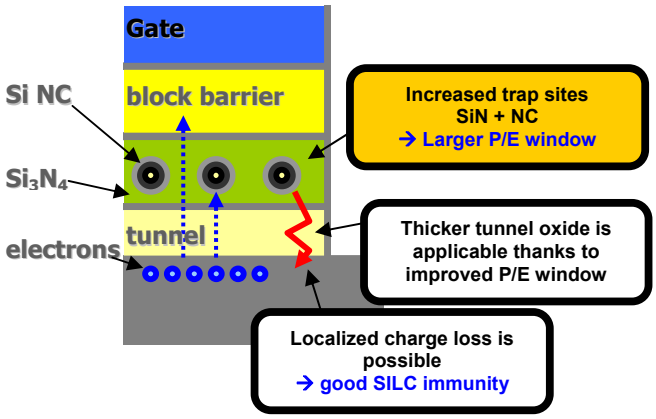


Fig. 1 Schematic diagram of proposed Hybrid trap layered NAND Flash device, illustrating the advantages of such structure

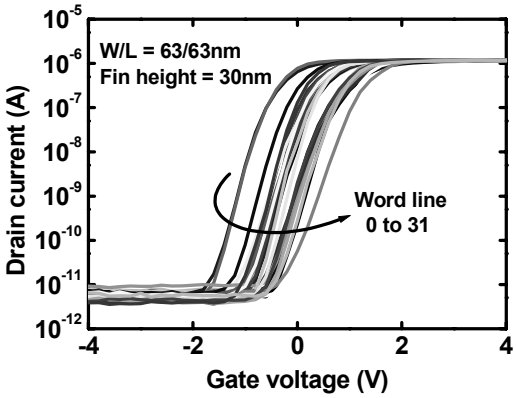
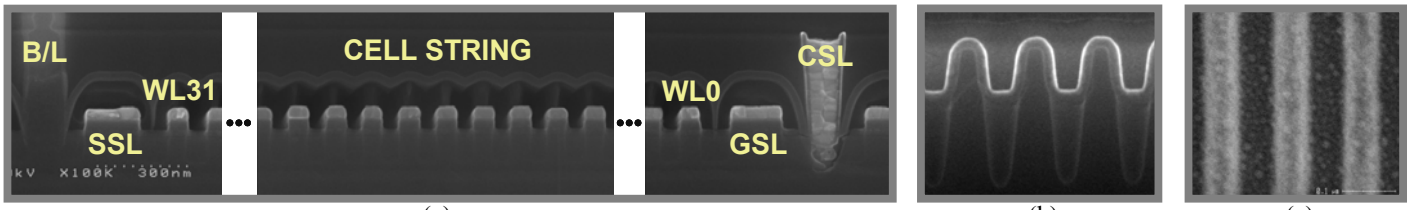
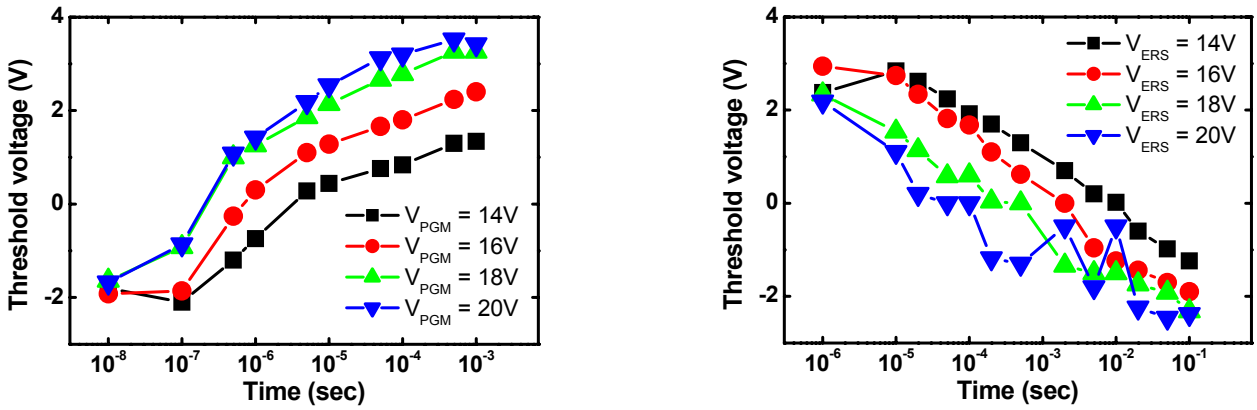


Fig. 3 Initial Id-Vg characteristics of 32 WL NAND string



(a) (b) (c)

Fig. 2 (a) Cross-sectional SEM view of fabricated NAND string, (b) FinFET cell structure, and (c) top view SEM image of Si nano-crystal on nitride layer



(a) (b)

Fig. 4 (a) Program and (b) erase transient characteristics of FinFET NAND Flash with hybrid trap layer. Forler-Nordheim tunneling is used both for the program and erase.

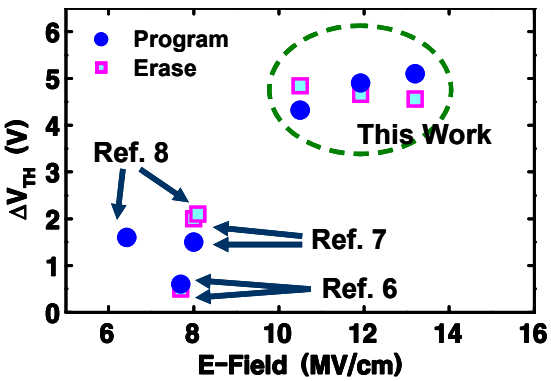


Fig. 6 Comparison of the program / erase window as a function of programming electric field, to the previous Si NC literatures.

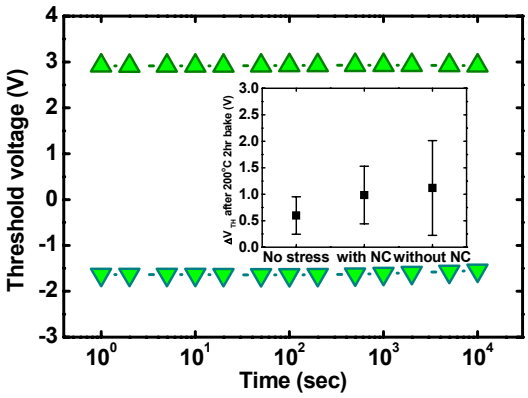


Fig. 6 Room temperature charge loss of programmed and erased memory cell. The inset shows the threshold voltage shift of 10 K cycled memory cell after 200 °C, 2 hour bake.