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2-Bit Lanthanum Oxide Trapping Layer Nonvolatile Flash Memory

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Abstract

This work demonstrates the 2-bit characteristics of SONOS-type memories by using high-κ dielectric materials Lanthanum oxide trapping layers. We use CHE programming and BTBHH erasing for the memory operation. Large memory windows, relative high P/E speed and good retention can achieve for SONOS-type memories. In summary, La_2O_3 are the candidates used for the trapping layers for the SONOS-type memories

Introduction

SONOS-type (poly – Si – oxide – nitride – oxide - silicon) structure memories have recently attracted much attention for the application in the next-generation nonvolatile memories [1] because of their great potential for achieving high program/erase speed, low programming voltage and low power performance. However, many concerning issues are still presented for both types of memories. In recent years, many papers have ever shown Al_2O_3 trapping layer as the potential candidate for replacing Si_3N_4 [2] and also demonstrated different kinds of high-k material to provide charge storage for the non-volatile memories.

In this paper, we have successfully achieved the high-k memories with Lanthanum oxide trapping layer. It has good characteristics in terms of considerably large memory window, high speed program/erase, good retention time, good endurance, and good disturbance.

Experimental

The fabrication process of the Lanthanum oxide memory devices was demonstrated with LOCOS isolation process on a p-type, 5-10 Ω cm, (100) 150mm silicon substrates. First, a 2nm tunnel oxide was thermally grown at 1000°C in vertical furnace system. Next, a Lanthanum oxide layer was deposited by E-gun method with Lanthanum oxide targets. After that, the samples went through RTA treatment in O_2 ambient at 900°C for 1 minute. A blocking oxide of about 8nm was then deposited by high density plasma chemical vapor deposition (HDPCVD) followed by 900°C 1 minute N_2 densification process. Then, poly-Si deposition, gate lithography, gate etching, source/drain (S/D) implant, substract contact patterning and the rest of the subsequent standard CMOS procedure were complete for fabricating the $La2O_3$ high-k memory devices.

Results and Discussion

Figure 1 shows the structure and process flow of the $La2O_3$ high-k memory. Figure 2 shows the cross-sectional HRTEM images of the gate stacks of La_2O_3 flash memories. The thicknesses of the tunnel oxide and blocking oxide layer are 2nm and 7nm. The trapping layer thickness is 4nm. Program characteristics as a function of pulse width for different operation conditions are shown in Fig. 3. Channel hot-electron injection (CHE) injection was employed for programming. With $V_d=V_g=10V$, relatively high speed (10μs) programming performance can be achieved with a memory window of about 2V. Meanwhile, Fig. 4 displays the erase characteristics as a function of various operation voltages. Band-to-band hot-hole (BTBHH) injection was employed for erasing. Again, erase speed of around 10 ms can be obtained with Vt shift of -2V.

The retention characteristics of the La_2O_3 memory devices at three temperature (T=25°C, 85°C, 125°C) are illustrated in Fig. 5. The retention time at 10^4 seconds has 7%, 11%, 18% charge loss at T=25°C, 85°C, 125°C, respectively. The endurance characteristics after 10^6 P/E cycles are also shown in Fig. 6. The programming and erasing conditions are $V_g=V_d=10V$ for 100μs and $V_g=-3V$, $V_d=10V$ for 10ms, respectively. Slight memory window narrowing has been displaye and the individual threshold voltage shifts in program and erase states become visible after 10^2 cycles. This indicates the formation of operation-induced trapped electrons. Certainly, this is intimately related to the use of ultra-thin tunnel oxide and minute amount of residual charges in the La_2O_3 layer after cycling.

The read disturb characteristics is shown in Fig. 7. Only tiny read disturbance emerges when $V_d < 4$ after 1000 seconds at 25°C. In addition, Fig. 8 and 9 shows the programming drain and gate disturb characteristics, respectively. After 1000 seconds at 25°C, < 1V drain disturb margin gate disturb margin are observed. Fig. 10 demonstrates the 2-bit operation with a single cell. Table 1 is the scheme of the bias conditions for the 2-bits/cell memory devices operation.

Conclusions

In this paper, we have investigated the memory effect on the performance of the La_2O_3 SONOS-type memories. It has good characteristics in terms of large memory windows, high speed program/erase, good retention time, excellent endurance, and 2-bit operation. Hence, La_2O_3 are the candidates used for the trapping layers for the SONOS-type memories.

References

[1] Peiqi Xuan, Min She, Bruce Harteneck, Alex Liddle, Jeffrey Bokor and Tsu-Jae King, "FinFET SONOS flash memory for embedded applications," in *IEDM Tech. Dig*., 2003, pp. 609-613.
[2]T. Sugizaki, M. Kobayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, "Novel multi-bit SONOS type flash memory using a high-k charge trapping layer," in *Proc. VLSI Symp. Technology Dig. Technical Papers*, 2003, pp. 27 - 28.

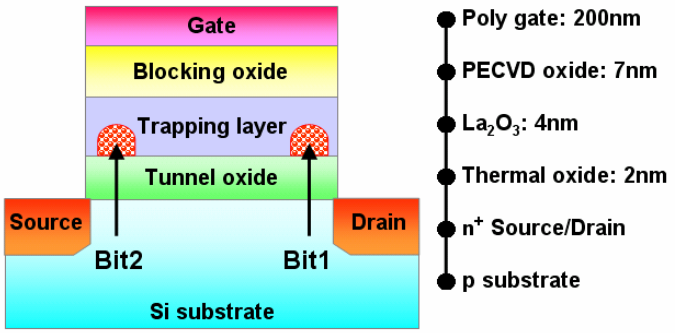

Fig. 1. Schematic cross section and process flow of La_2O_3 memory device.

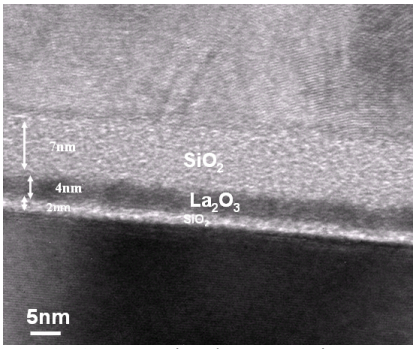

Fig. 2. Cross-sectional HRTEM images of the gate stacks for the SONOS-like memories with La_2O_3 trapping layers.

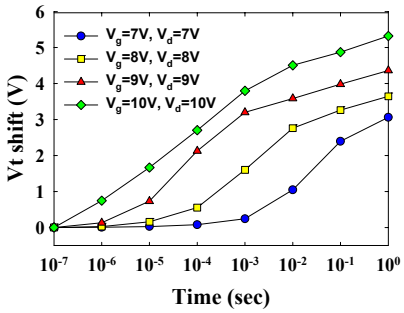

Fig. 3. Program characteristics of La_2O_3 memory device with different programming conditions.

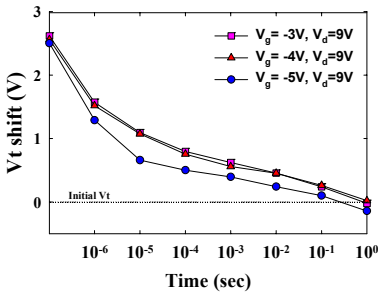

Fig. 4. Erase characteristics of La_2O_3 memory device with different erasing conditions.

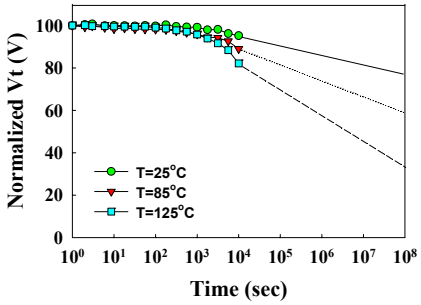

Fig. 5. Retention characteristics of La_2O_3 memory at T=25°C, 85°C, 125°C.

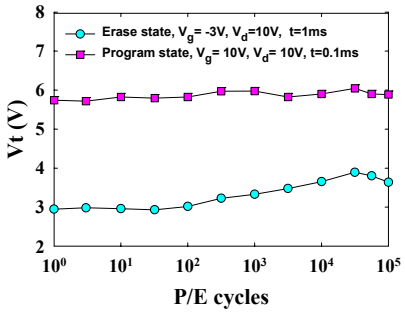

Fig. 6. Endurance characteristics of La_2O_3 memory device. Negligible degradation is found even after 10^6 P/E cycles.

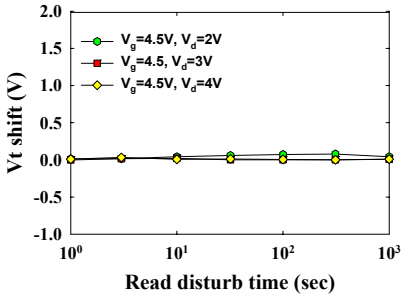

Fig. 7. Read disturb characteristics with no significant V_t shift when V_d<4 even after 1000 seconds at 25°C.

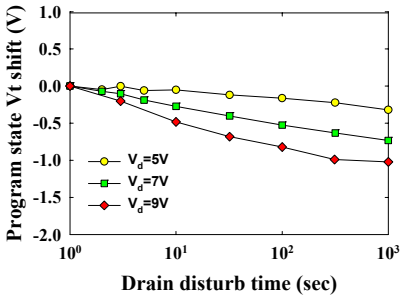

Fig. 8. Programming drain disturb characteristics with different voltages.

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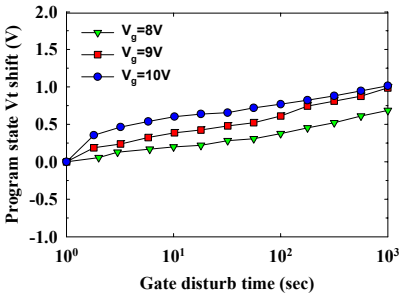

Fig. 9. Gate disturb characteristics with different voltages.

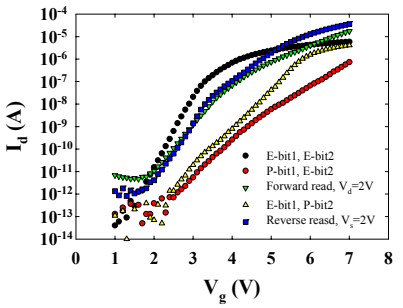

Fig. 10. Demonstration of 2 bits/cell operation.

		Program	Erase	Read
Bit 1	Vg	10V	-3V	4V
	Vd	10V	10V	0V
	Vs	0V	0V	>3V
Bit 2	Vg	10V	-3V	4V
	Vd	0V	0V	>3V
	Vs	10V	10V	0V

Table 1. Suggested bias conditions for the 2 bits/cell memory operation.