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A Novel NAND Flash Technology with Selective Epitaxial Growth Plug Structure for the Improvement in HV Transistor Breakdown Voltage

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Abstract

In this article, we demonstrate successful integration of selective epitaxial growth (SEG) contact for high density NAND flash memory devices. For high transistor breakdown voltage of a scaled high voltage (HV) transistor, SEG process was adopted to prepare for elevated doped region. It was found that the plug ion implantation (IIP) as a key step should be differently applied to HV transistor region and cell region. By employing optimized SEG contact in scaled NAND flash devices, HV transistor breakdown voltage, comparable Id-Vg characteristics, body effect, shut off and isolation characteristics were obtained without any noticeable degradation of cell characteristics.

Introduction

For the past 10 years, much effort has been dedicated to scale NAND flash memory devices [1, 2]. However, even with various junction structures such as lightly doped drain (LDD) structure and DDD (doubly doped drain) structure [3, 4], the aggressive scaling of HV transistor was a formidable task. There are limits on manufacturing more highly integrated devices capable of resisting high voltages using such junction structures. To overcome a short channel effect, the scaling of a low concentration junction depth causes the degradation in junction breakdown. To obtain high junction breakdown, an effective area of the high concentrated diffusion layer should be increased.

An elevated source and drain technology has thus been developed with an epitaxial layer formed on a substrate and impurities being implanted into the epitaxial layer [5]. In our study, we address a successful integration of the SEG process into HV transistor fabrication for high density NAND flash with design rule of 63nm and beyond.

Experimental

Fig. 1 shows the integration scheme to implement SEG process for HV transistor contact and cell bit line contact in 63nm technology. After gate stack processes, all devices were capsulated by inter-dielectric, followed by forming contact holes by dry etch process. Then, SiN sidewall spacers of contact holes were formed to increase the growth rate of the subsequent epitaxial layer. Plug IIP was performed on the only cell region because of different requisite of plug IIP for peripheral HV transistor region and cell region. Afterward, the epitaxial layer in both regions was deposited simultaneously by SEG method, followed by IIP on epitaxial layer. As a contact metal and bit line material, W layer was subsequently deposited and patterned.

Results & Discussion

Fig. 2 compares device structures of a conventional HV transistor with doped poly-Si direct contact (DC) and a novel HV transistor with SEG contact. By implementing elevated source and drain by SEG, the lateral distance from gate to contact can be decreased from A (conventional HV Tr.) to B (novel HV Tr.). Fig. 3 shows the simulation results of gate induced drain leakage (GIDL) current of conventional HV Tr., and novel HV Tr. Compared to a conventional HV Tr., a novel HV Tr. device shows reduced GIDL at high drain bias, resulting in improved transistor breakdown voltage because of the increased effective gate to contact distance from A to A plus α. Fig. 4 & 5 show different requirements of plug IIP for HV transistor region and cell region. There is little difference between a conventional HV device with plug IIP plus doped poly-Si DC and a novel HV device with plug IIP plus SEG contact. However, the novel HV device without plug IIP process shows high transistor breakdown voltage up to 3.7V. Therefore, the plug IIP should be skipped for HV device with SEG contact. However, in terms of worst-on-cell-current, plug IIP prior to SEG process is favorable. Fig. 6 shows the Id-Vg characteristics of a novel HV Tr. with IIP dose on top of the epitaxial layer. In our experiments, IIP condition was variously optimized. The current characteristics of optimized SEG contact were comparable to conventional one at the same effective gate to contact distance (lateral plus vertical). Fig. 7 shows high transistor breakdown voltage characteristics for SEG contact device regardless of the distance from gate poly to contact without any degradation of other electrical characteristics including body effect in Fig. 8, virgin V_{th}, shut off and isolation characteristics (not shown). Fig. 9 shows the junction characteristics implemented by conventional DC and SEG contact. The SEG contact shows lower junction leakage and higher breakdown voltage, which can be explained by the increased resistive layer. Fig. 10 shows measured worst-on-cell-current of SEG contact device and conventional contact device with V_{read} of 5.5V, and 6V. No degradation was observed in the measured worst-on-cell-current at V_{read} of less than 5.5V. Considering of low V_{read} condition for multi level, the measured worst on cell current at 5.5V is acceptable.

Summary

In our study, we address a successful integration of SEG process into HV transistor fabrication for high density NAND flash process technology with design rule of 63nm and beyond. For high transistor breakdown voltage of a scaled HV transistor, SEG process was adopted to prepare for elevated doped region. The plug IIP as a key step should be differently applied to HV transistor region and cell region. By employing optimized SEG contact in a scaled HV transistor, high transistor breakdown voltage, comparable Id-Vg characteristics, body effect, shut off and isolation characteristics were obtained without any noticeable degradation of cell characteristics.

References

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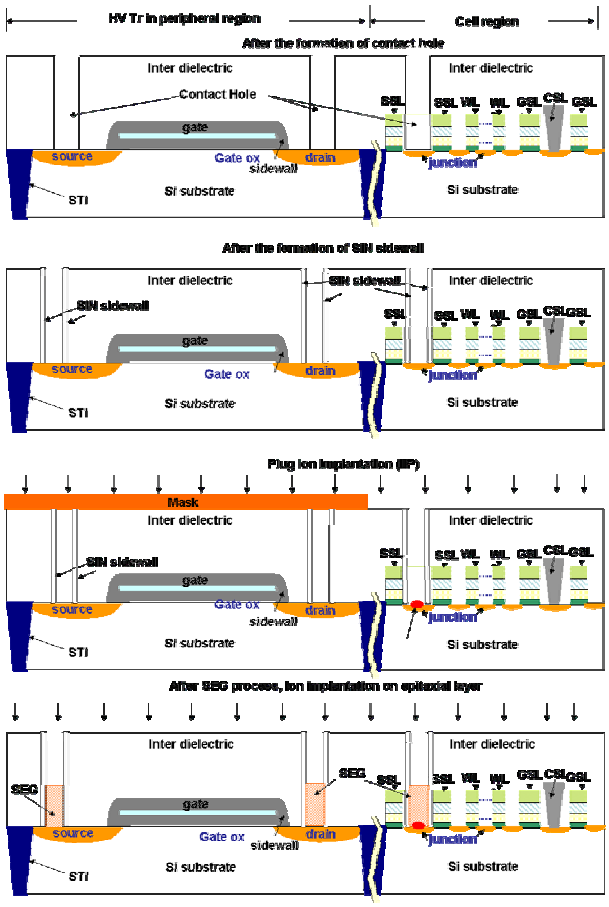

Fig.1. Integration scheme. After forming contact holes by dry etch process SiN sidewall spacers of contact hole were formed to increase the growth rate of subsequent epitaxial layer. Plug IIP was performed only on the cell region, followed by SEG process and ion implantation on epitaxial layer

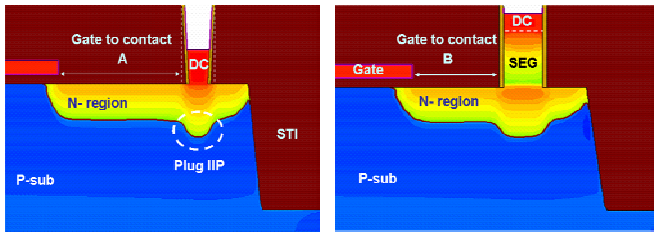

Fig 2. (Left) Conventional HV transistor. with direct contact (DC). (Right) Novel HV transistor with elevated source and drain (ESD) by Selective Epitaxial Growth (SEG)

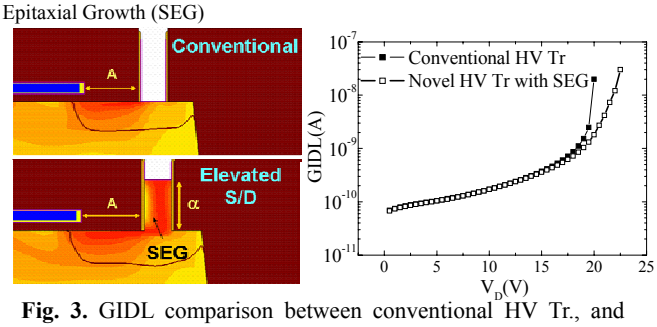

Fig. 3. GIDL comparison between conventional HV Tr., and novel HV Tr. with SEG (Simulation results)

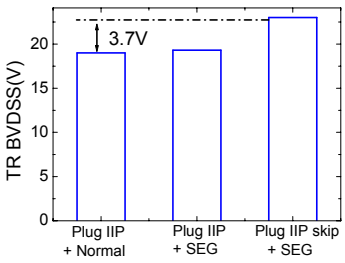

Fig. 4. Measured TR BVDSS of conventional HV Tr. and novel HV Tr. w/ & w/o plug IIP process

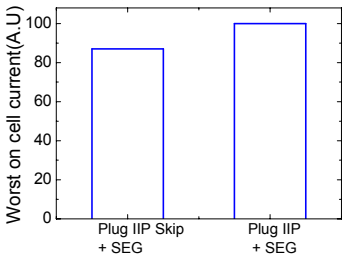

Fig. 5. Measured worst-on-cell-current of novel HV Tr. w/ and w/o plug IIP process

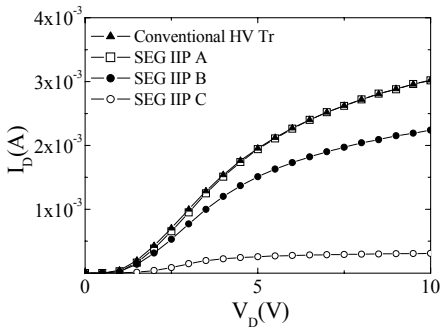

Fig. 6. Id-Vd characteristics of conventional HV Tr., and novel HV Tr. with IIP dose on epitaxial layer @ same effective gate to contact distance (lateral plus vertical)

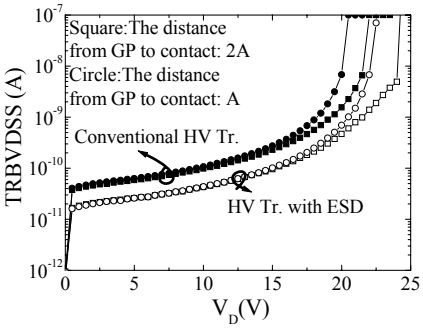

Fig. 7. TR BVDSS of conventional HV Tr and novel HV Tr. with respect to the distance from gate poly-Si to contact (lateral only)

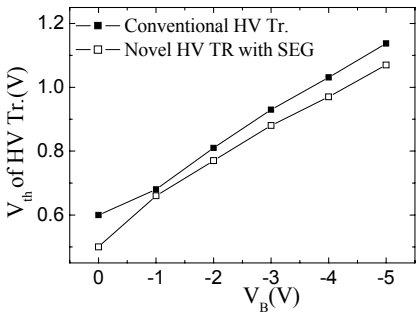

Fig. 8. Body effect of conventional HV tr and novel HV Tr. with SEG

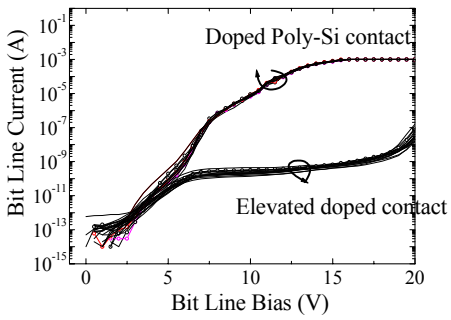

Fig. 9. Cell junction characteristics between doped poly-Si contact and elevated doped contact by SEG (Left figure)

Fig. 10. Worst-on-cell-current between elevated doped contact (SEG contact) and doped poly-Si contact (DC) with respect to V read bias of 5.5V, and 6V, (Right figure)