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Low Power Spin-Transfer MRAM Writing Scheme with Selective Word Line Bootstrap

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1. Introduction

Magnetoresistive random access memory (MRAM) is one of the emerging nonvolatile memories with features such as fast read and write access time, high density, and high endurance [1]. However, large power consumption due to the writing current prevents the realization of high density MRAM. Spin-transfer switching (STS) [2] is one of the solutions of such problem, which reduces both the writing current and memory cell area. The spin-transfer switching in magnetic tunnel junction (MTJ) with size of deep submicron was already demonstrated [3], [4], therefore it can replace the conventional current induced magnetic field switching MRAM due to the low write current.

While spin-transfer MRAM cell structure can be simplified due to eliminating the write word line, writing current has to pass through the cell transistor. Therefore, gate width of the cell transistor depends on the magnitude of the writing current. On the other hand, required bit line cramp voltage which can provide enough writing current is not constant. As it depends on the stored data, MTJ characteristics, and current direction, it has to be optimized to minimize the power consumption.

In this study, we present a new writing scheme for spin-transfer MRAM with selective word line bootstrap, which realizes a low power operation. In addition, the spin-transfer MRAM cell was modeled for the circuit simulation.

2. Spin-Transfer MRAM Cell Modeling for Read and Write operation

A model for MTJ resistance was developed for the circuit simulation. Both reading and writing models are embedded into a commercial standard SPICE simulator such as Eldo [5], and then operation of the spin-transfer MRAM can be simulated.

Regarding the reading behavior [6], I/V and R/V characteristics were simulated using the following Simmons tunneling formula with spin direction ϕ, as shown in Fig. 1 [7].

$$MR(V) = C_1|V|^3 + C_2|V|^2 + C_3|V| + C_4 \quad (1)$$

$$R(V,\phi) = \frac{r}{S}\left(1 + \frac{MR(V)}{100}\cos\frac{\phi}{2}\right) \quad (2)$$

$$I(V,\phi) = \frac{1}{R(V,\phi)}\left(V + \gamma_s V^3\right) \quad (3)$$

In these formula, $R(V, \phi)$ stands for the MTJ resistance which is represented by (2). S stands for the MTJ area, and r is the minimum MTJ resistance per unit area. $MR(V)$ is the MR ratio dependence on MTJ bias voltage V, which is obtained by polynomial approximation. Coefficients of C_1, C_2, C_3 and C_4 in (1) are determined from experimental results [8], [9].

Regarding the writing behavior, the spin direction follows LLG equation (4) with a spin torque transfer term [2].

$$\frac{dS_2}{dt} = \gamma S_2 \times H_{eff} - \alpha \hat{s}_2 \times \frac{dS_2}{dt} - g\frac{I_e}{e}\frac{\hbar}{2}\hat{s}_2 \times \left(\hat{s}_2 \times \hat{s}_1\right) \quad (4)$$

In the above equation, S_2 is the spin angular momentum of free layer, $\hat{s}_1$ is the transferred spin direction with constant value, γ is the electron gyromagnetic ratio, H_{eff} is the external magnetic field, α is the Gilbert dumping constant, g is the spin transfer efficiency, and I_e is the current through MTJ. From this equation, threshold current, which can change the spin direction with spin torque transfer, can be expressed by the equation (5).

$$I_e = 2\alpha\gamma H_{eff} e S_2 / g\hbar \quad (5)$$

From such MTJ resistance model including both bias voltage and spin direction dependence, spin-transfer MRAM cell operation can be successfully simulated with high accuracy.

3. Configuration of Proposed Writing Scheme with Selective Word Line Bootstrap

Configuration of the spin-transfer MRAM cell circuit and simulated I/V characteristics are shown in Fig. 2. It is quite obvious that the write threshold voltage is different between forward and reverse bias, and also clear that the difference is larger than that of the MTJ shown in Fig. 1. While the forward current depends on a voltage V_{word}-V_{th}, where V_{word} is the word line voltage and V_{th} is the cell transistor threshold voltage, IR-dropping of the MTJ affects the reverse current in addition to these voltages. On the other hand, the bit line cramp voltage is limited to prevent the junction destruction of the MTJ and the increasing of the writing power consumption. Therefore, the difference of the write threshold voltage should be decreased.

To solve this problem, our proposal is to change the word line voltage in accordance with the write current direction. Configuration of the proposed word line driver for the selective word line bootstrap is shown in Fig. 3. It consists of a level shifter with bootstrap voltage V_b and voltage select pass gates.

4. Simulation Results and Discussions

Circuit simulation has been applied using 0.1 μm SOI CMOS technology [10] to confirm the proposed writing scheme. Simulation parameters are listed in Table I. The write threshold bit line voltage with the reverse current direction has been simulated for each word line bootstrap voltage. The gate width of each cell transistor was minimized to suppress the memory cell area. Figure 4 shows the writing simulation results with various threshold current,

resistance, and MR ratio. The write threshold bias was decreased from 17 to 28% under 1.5V bootstrap voltage. These results reveal that the proposed writing scheme can successfully suppress the bit line voltage during the writing operation.

5. Conclusions

The low power writing scheme with selective word line bootstrap for spin-transfer MRAM was proposed, and its effect was successfully confirmed by circuit simulation. Furthermore, the spin-transfer MRAM cell modeling was implemented for the simulation. From the simulation result, write threshold bit line bias during the writing operation can be decreased from 17 to 28% with the proposed selective bootstrap. The proposed writing scheme can proceed the realization of low power and high performance MRAM.

Acknowledgment

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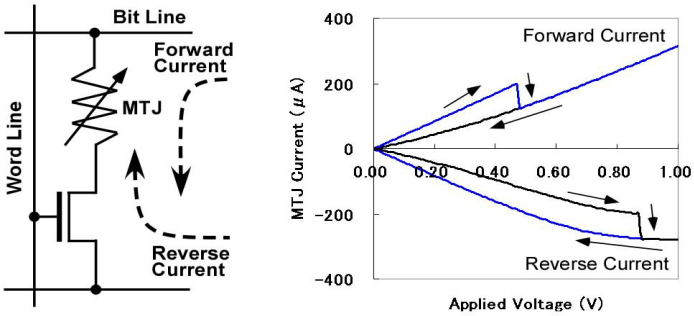
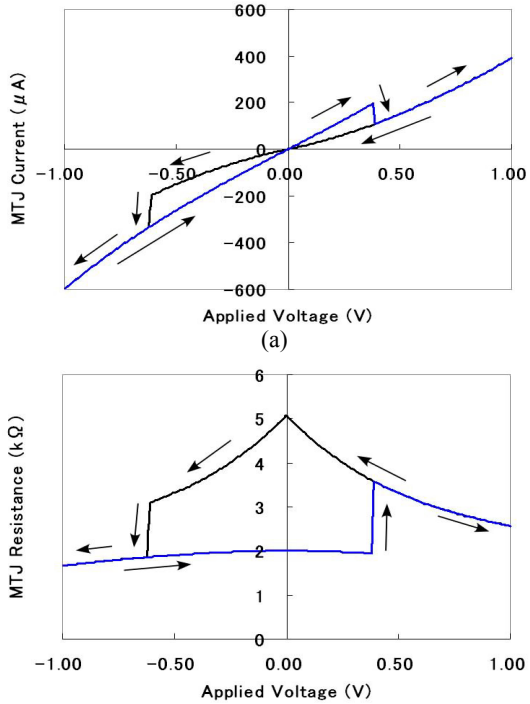


(a) (b)

Fig. 2. Configuration of the memory cell circuit and simulated I/V characteristics. (a) Spin-transfer MRAM cell circuit. (b) I/V curves for the series of a MTJ and a cell transistor. (Rmin=2kΩ, MR=150% at 0V, Ith=200μA, Vword=1.2V)



(a) (b)

Fig. 1. Simulated I/V and R/V characteristics with spin-transfer MRAM reading and writing model. (a) I/V curves. (b) R/V curves. (R_{min}=2kΩ, MR=150% at 0V, I_{th}=200μA)

Table I. Simulation parameters.

Power Supply (V)	1.2
Technology	0.1μm SOI CMOS [10]
MTJ resistance (kΩ)	1.0-2.0
MR ratio (%)	100-300 at 0V
Threshold current (μA)	100-200
Bootstrap voltage (V)	1.2-1.5

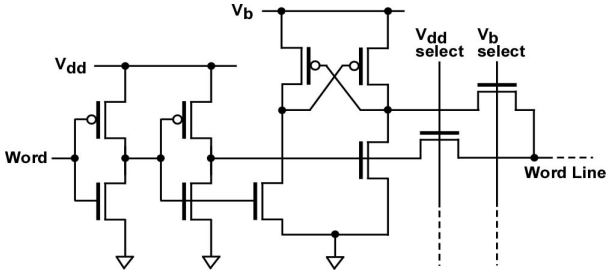
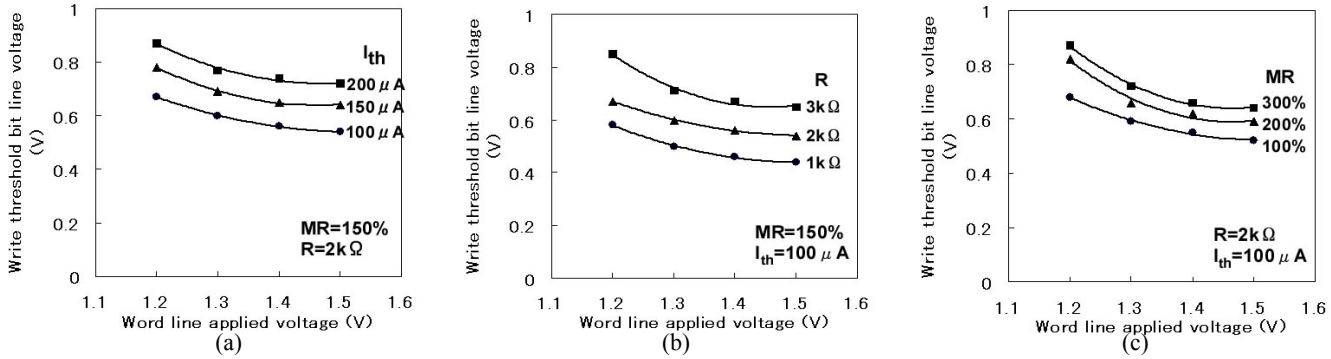


Fig. 3. Word line driver for proposed selective bootstrap.



(a) (b) (c)

Fig. 4. Simulation result of writing operation with selective word line bootstrap. (a) Simulation result for various threshold write current. (b) Simulation result for various MTJ resistance. (c) Simulation result for various MR ratio.