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A Novel Open-Loop High-Speed CMOS Sample-and-Hold

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1. Introduction

As demand for very high speed high resolution CMOS ADCs grows, more and more highly linear high speed S/H circuits are required. Due to inherent limitations of feedback structures, S/Hs based on feedback no longer can satisfy the speed needed [1]. The dominant way around it has been passive S/Hs which lack any buffering capability [2]. This mandates ADCs to employ architectures based on switched-capacitor circuits. Despite being rather simple, the switched capacitor blocks (internal DAC, gain stage, etc), and hence the implemented ADC, cannot achieve the highest speed that a given process potentially offers. Previously, an open-loop S/H was introduced. However, its linearity was rather limited. In this article we describe a new S/H which maintains high speed while much improves linearity.

2. Open Loop S/H with Input Switch Sampling

Fig. 1 shows simplified half circuit diagram of a basic open-loop differential CMOS S/H circuit. Even assuming ideal buffers, because of voltage dependent charge injection of input switches, the circuit exhibits very poor linearity despite partial improvement by dummy switches. The first reason is that there is a random mismatch between sampling and dummy switch pairs. More important reason is that even for perfectly matched sampling and dummy switch pairs, perfect cancellation of charge injection is not guaranteed. Since sampling switch charge (when it opens) is divided depending on, among others, impedance it sees from each side, and rise/fall time of switch's driving signals. To alleviate this problem, the ground plate sampling is used as a solution (Fig. 2). However, despite its advantages over S/H of Fig. 1, the circuit of Fig. 2 suffers from the same voltage-dependent charge injection, as in Fig. 1.

3. Open Loop S/H with Ground Plate Sampling

Fig. 2 shows the open loop S/H with grounded plate sampling. It is argued that a single differential switch M0 functions as a perfect differential sampler, always operates at ground potential, and creates fixed equal charge injection on both sides. Plus, input switches M2 and M5 do not cause any charge injection provided that M0 is connected to top plates of the holding capacitors. The argument is based on that "there is no path for charge injection by input switches, when they open after sampling switch," which is not valid. As shown in Fig. 2, always there are parasitic capacitors Cp at nodes A1 and A2. Those are drain diffusion capacitors of M0, M1, and M4. Hence, when input switches open, there are series Ch||Cp capacitors providing paths for charge injection, exactly as in Fig. 1. Charge injection on each side is input voltage dependent causing odd harmonics at the least.

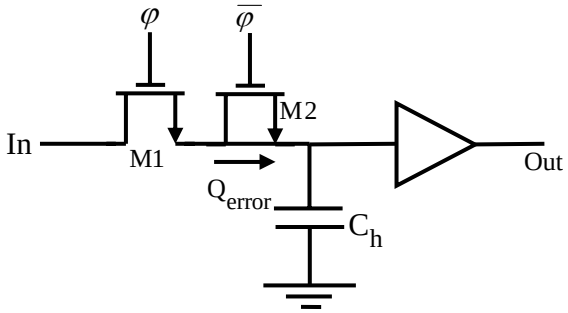

Fig. 1 Half circuit diagram of a basic open loop S/H

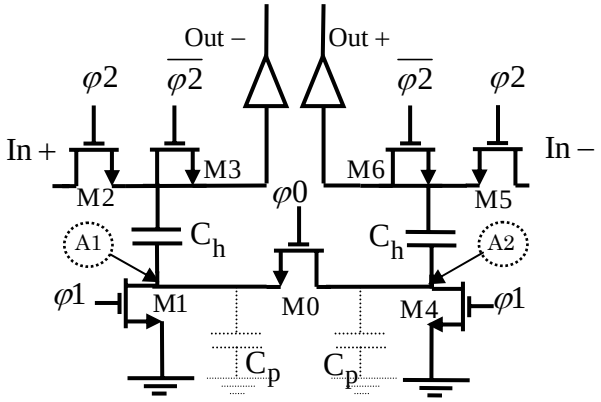

Fig. 2 An open loop S/H with bottom plate sampling

Smaller Ch||Cp than Ch might reduce charge injection but does not eliminate it. If α is the uncancelled fraction of charge, then the differential error voltage due to charge injection is

$$V_{error,1} = \alpha(Vin + \Delta V_{th})C_{ox}WL \times \frac{1}{2C_h}$$

4. New S/H with Auxiliary Capacitors

Fig. 3 shows schematic diagram for the new open loop CMOS S/H. The buffers, Fig.4, are source followers with single device current sources proved in [4], for best linearity. The difference with the S/H in Fig. 2 is that there are two auxiliary capacitors which drastically reduce effect of input switches' charge injection in sampled and output signals. Fig. 5 shows clock sequence for different switches. Here, when input sampling switch M0 opens, there remain two capacitors on each side to absorb injected charge residue by input switches. One is series cap Ch||Cp and the other is Ch'. Ch and Ch' are in the same order while parasitic Cp is much smaller. Hence only a small fraction of the residue charge injection is absorbed by Ch. Later, first M2 and M5 open and then M1 and M4 are closed, leaving effect of only a fraction of residue charge injection on the sampled and output signals.

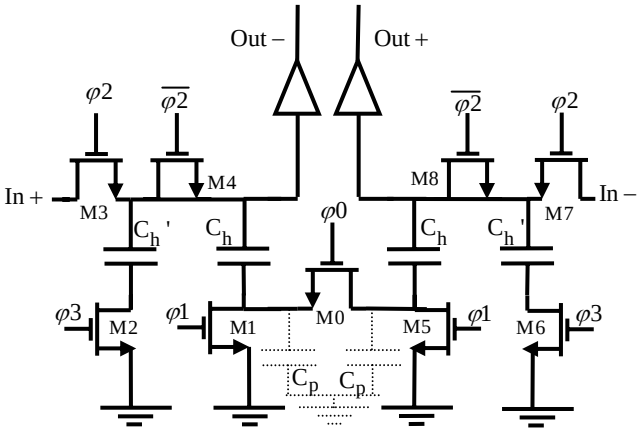

Fig. 3 New open loop S/H with auxiliary capacitors

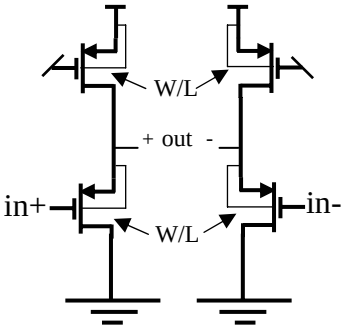

Fig. 4 Buffer used in S/H

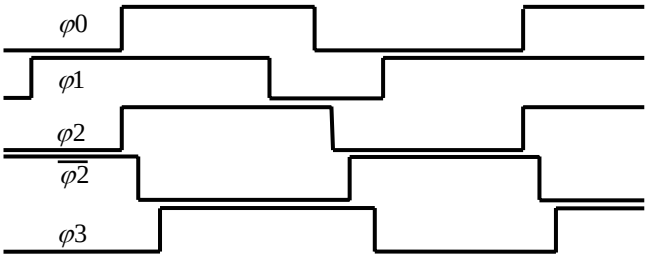

Fig. 5 Clock signals of the new S/H circuit

Then charge injection error voltage becomes

$$V_{error,2} = \alpha(Vin + \Delta V_{th})C_{ox}WL \times \frac{C_p \| C_h}{2(C_h' + C_h \| C_p)^2}$$

indicating a dramatic reduction of charge injected error.

5. Simulation Results

To evaluate the concept, two S/Hs of Fig. 2 and Fig. 3 were designed in a 0.35um double poly CMOS process. Single ended loads of each S/H are 1pF, while holding capacitors are 0.5pF each. Total current for each case is 0.6mA. The two circuits were simulated in identical conditions. Sinusoidal signals of 1.6 Vp-p with frequencies of 1.7, 20 and 40MHz were applied to both S/Hs. Sampling frequencies were 250MHz and 500MHz. The output spectra for the case of 20MHz input and clock rate of 250MHz are shown in Fig. 5 and Fig. 6 for the new S/H and that of Fig. 2, respectively. The results are summarized in Table 1. It is seen that in every case there is at least about 10dB improvement in SNDR.

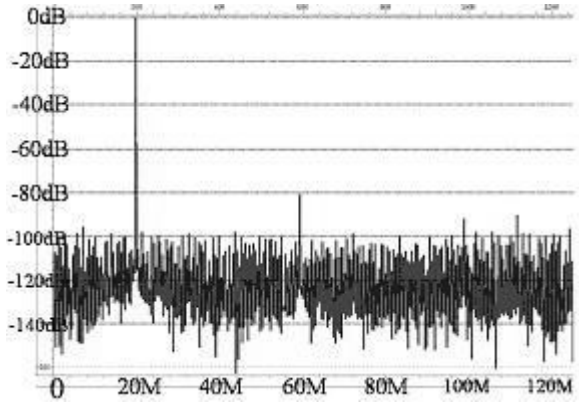

Fig. 5 New S/H output spectrum for 20MHz input, 250MHz clock

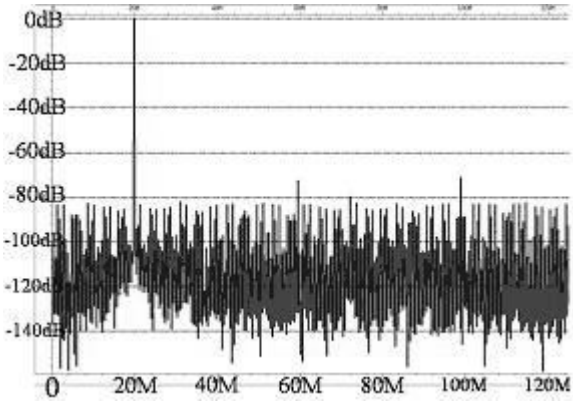

Fig. 6 Output spectrum of Fig. 2 for 20MHz input, 250MHz clock

Table1 Dynamic performance of the new S/H and [3]

Sampling Rate		250 (MHz)			500 (MHz)	
Input Freq.		1.7	20	40	20	40
This Work (dB)	HD3	-83	-79	-76	-79	-74.3
	HD5	-105	-96	-89	-92	-81
	SNDR	79	76.8	70	75	69
Work in [3] (dB)	HD3	-82	-80	-77	-83	-80
	HD5	-70	-72	-74	-74	-72
	SNDR	68	64	60	63	59.7

6. Conclusions

A new method for further reduction of voltage dependent charge injection was presented. Based on the concept a new S/H was designed which shows over 10 dB improvement in SNDR compared to S/H of [3]. The concept can be also implemented in other open loop schemes.

References

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