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Constant Magnetic Field Scaling in Inductive-Coupling Data Link

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1. Introduction

A wireless transceiver utilizing inductive coupling has been proposed ([1-3]) for System in a Package (Fig. 1). The transceiver communicates at 1Gbps/channel between stacked chips [1]. By arranging the transceivers in a channel array, 195Gbps [2] and 1Tbps [3] data bandwidth is achieved. This paper discusses scaling theory based on constant magnetic field. The theory is verified by simulation and measurement results in 0.35, 0.25, 0.18μm and 90nm CMOS.

2. Theory for Inductive-Coupling Data Link

In the inductive-coupling data link, a transmitter changes transmit current I_T in a transmitter inductor according to data and a receiver senses induced voltage V_R to recover the data. V_R is given by

$$V_R=M(dI_T/dt)=kL(dI_T/dt) \quad (1)$$

where M is a mutual inductance between the inductors and k is a coupling coefficient. k denotes how much magnetic flux reaches between the inductors therefore k is mainly determined by physical shape such as inductor diameter and vertical distance. L is a self inductance of the transmitter and receiver inductor (same inductor is used for both transmitter and receiver) which is approximately given by

$$L=L_0n^2D^{1.5} \quad (2)$$

where L_0 is a self inductance of 1 turn inductor at a unit area, n is a number of turns, D is a diameter of the inductor. Validity of Eq.(2) will be verified by simulation and measurement results in Section 4. In addition, dI_T/dt can be approximated by

$$dI_T/dt=I_D/t_{pd} \quad (3)$$

where I_D is drain current and t_{pd} is propagation delay. As a result, V_R is given by

$$V_R = kL_0n^2D^{1.5} I_D/t_{pd}. \quad (4)$$

3. Constant Magnetic Field Scaling

Even when channel is scaled down, V_R should be constant to maintain a bit error rate. Figure 2 summarizes scaling factors in Eq. (4). The transistor size and supply voltages are scaled by $1/\alpha$ with maintaining I_D/t_{pd} constant [4]. By thinning chip thickness T to reduce communication distance X, k remains constant if the inductor is scaled down by $1/\alpha$ because of constant magnetic field. Also crosstalk condition will not be degraded. Since L_0 is constant, if $n^2D^{1.5}$ in Eq. (4) is also constant, V_R becomes constant. To keep $n^2D^{1.5}$ constant value, n should be increased by $\alpha^{0.75}$ (to simplify, it is expressed $\alpha^{0.8}$ in this paper). n can be increased by utilizing increased number of metal layers. Finally, by the scaling, aggregated bandwidth per area will be increased and energy per bit will be reduced by a factor of α^3.

4. Simulation and Measurement Results

In Eq. (4), L_0 and I_D/t_{pd} are constant so that the proposed scaling theory is verified when k and $n^2D^{1.5}$ are constant.

At first, it is confirmed by a simulator [5] that k becomes constant when the inductor's diameter and the chip thickness are scaled down simultaneously. To confirm this assumption one turn inductors are simulated by varying scaling parameter D, T, w. Figure 3 shows the result where horizontal axis expresses communication distance and the solid line expresses k. w is assumed to $D/10$ for simplification. In this figure, for example, a k value where D/X becoming 2 are k=1.8 in α=1 (D=300μm), k=1.8 in α=2 (D=150μm), k=1.8 in α=3 (D=100μm), and so on. This result shows that k becomes constant value if D, X, (w) are scaled down with same rate.

Next, it is confirmed by the simulator that the term $n^2D^{1.5}$ becomes constant value in scaled inductor. This result is shown in Fig. 4. Simulated inductor has parameters that D=300μm, n=1 when α=1 and α is increased to 10. As shown in Fig. 4, $n^2D^{1.5}$ agrees very well to the simulated result. This result shows that proposed scaling rule is correct.

The proposed scaling theory is verified by measurement results. Figure 5 shows scaling parameters of the inductors utilized for previously fabricated chips [1-3] in 0.35, 0.25, 0.18μm CMOS and a newly-developed chip in 90nm CMOS. These inductors have a parameter which dose not follow scaling rule perfectly. But the ratio of $L/(L@0.35)$ and $n^2D^{1.5}/(n^2D^{1.5}@0.35)$ well agree with each other.

Frequency characteristics of inductor become problem in scaled inductor. In this paper, single pulse communication is assumed. If center frequency of signal is near to the resonant frequency of inductor, inter signal interference is getting worse. The pulse's center frequency and resonant frequency should be part enough to maintain good bit error rate. Figure 6 shows the resonant frequency and maximum frequency of pulse generation circuit which is used at transmitter in paper [2]. In this figure, inductors have a same parameter as shown in Fig. 5. This graph shows that the resonant frequency is higher more than pulse's maximum frequency. From this result, the resonant frequency will not become an issue in scaled inductor.

5. Conclusions

A constant magnetic field scaling for inductive coupling data link is discussed. It indicates that the bandwidth per area will be increased and energy per bit will be reduced by a factor of α^3 when the chip thickness is reduced as technology is scaled by α. Simulation and measurement results have good agreement with the theory.

References

[1] D. Mizoguchi, *et al.*, "A 1.2Gb/s/pin Wireless Superconnect based on Inductive Inter-Chip Signaling (IIS)," *ISSCC Dig. Tech. Papers*, pp.142-143, Feb. 2004.

[2] N. Miura, et al., "Analysis and Design of Inductive Coupling and Transceiver Circuit in Inductive Inter-Chip Wireless Superconnect," *JSSC*, vol. 40, No. 4, Apr. 2005, pp.829-837.

[3] N. Miura, et al., "A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link," *ISSCC Dig. Tech. Papers*, pp.424-425, Feb. 2006.

[4] D. Dennard, et al., "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," *JSSC*, vol. Sc-9, No. 5, Oct. 1975, pp.256-267.

[5] ASITIC web site: http://rfic.eecs.berkeley.edu/~niknejad/asitic.html

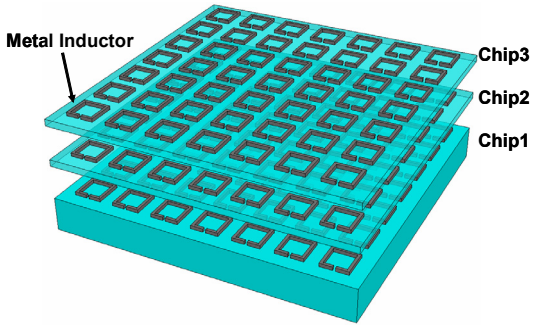

Fig. 1. Inductive-coupling data link.

Transistor Size	[x]	1/α
Power Supply Voltage	[V]	1/α
Chip Thickness	[T]	1/α
Coil Turn Number (Layer #)	[n]	$\alpha^{0.5}$
Current	[I_T]	1/α
Circuit Delay Time	[t_{pd}]~[CV/I_T]	1/α
Coil Diameter	[D]~[1/x]	1/α
Self Inductance	[L]~[$n^2D^{1.5}$]	1
Magnetic Coupling Coefficient	[k]	1
Receive Signal	[V_R]~[$kn^2D^{1.5}(I_T/t_{pd})$]	1
Crosstalk	[V_{RS}/V_{RN}]	1
Data Rate / Channel	[1/t]	α
Channel Number / Area	[$1/D^2$]	α^2
Aggregated Data Rate / Area	[$1/tD^2$]	α^3
Energy / Bit	[$I_T t_{pd}/V$]	$1/\alpha^3$

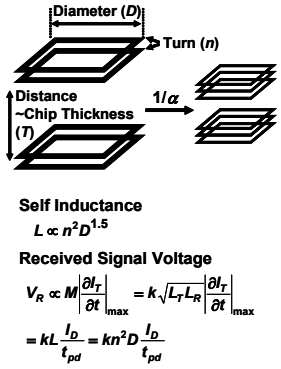

Fig. 2. Constant magnetic field scaling.

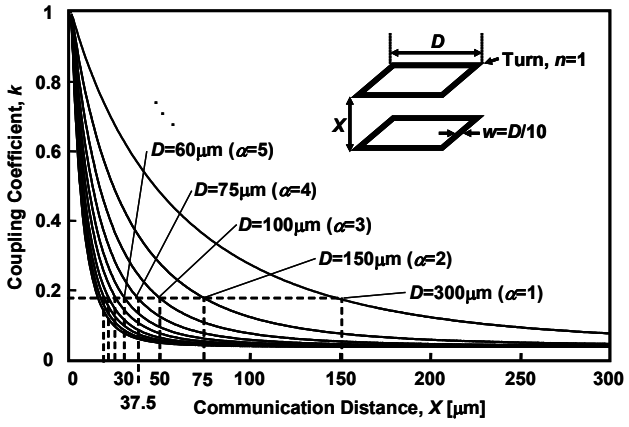

Fig. 3. Simulated coupling coefficient dependence on communication distance and diameter.

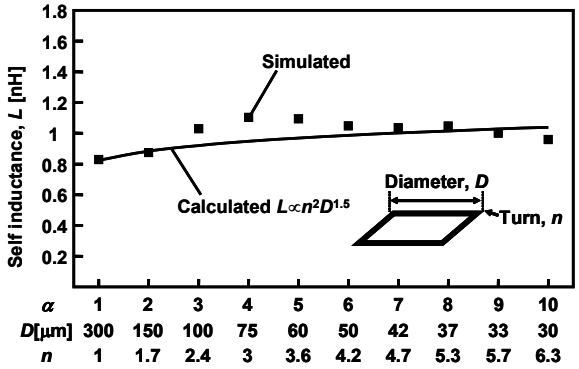

Fig. 4. Simulated and calculated self inductance.

Chip Micro-Photograph	[1]	[2]	[3]	
Process[μm]	0.35	0.25	0.18	0.09
α	1	1.4	1.9	3.9
D [μm]	300	48	30	20
X [μm]	50	15	15	15
n	2	4	4	4
V_{DD} [V]	3.3	2.5	1.8	1.0
E/bit [pJ]	46	6	3	0.5
L/(L@0.35)	1	0.59	0.29	0.15
SC/(SC@0.35)	1	0.57	0.28	0.15

$SC=n^2D^{1.5}$

Fig. 5. Scaling parameters in fabricated chips.

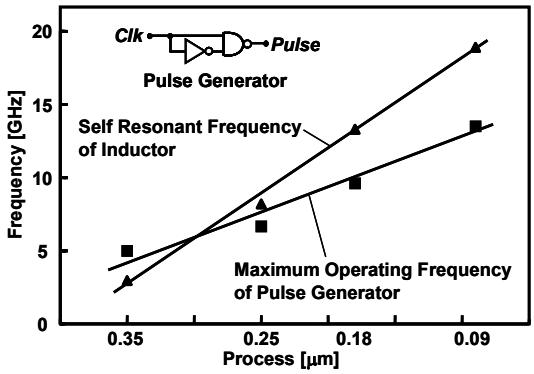

Fig. 6. Simulated self resonant frequency and maximum operating frequency of pulse generator depending on process.