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Investigation of Analog Performance for Uniaxial Strained PMOSFETs

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1. Introduction

To enable the mobility scaling, process-induced strained silicon has been widely used in state-of-the-art CMOS technologies [1,2]. Although the carrier mobility enhancement can help overcome the speed/power barrier for logic applications, the impact of strain on analog performance is not well known and merits investigation. Important metrics for analog applications include g_m/I_d, output resistance (R_{out}), dc gain (g_mR_{out}), and the gain-bandwidth product. Through a comparison between strained and control devices, this work examines the analog performance in uniaxial strained PMOSFETs [2] with sub-100 nm gate length.

2. Devices and Intrinsic I_d Extraction

The devices used in this study were fabricated by state-of-the-art process-induced uniaxial strained-Si technology [3]. Since the source/drain series resistance (R_{sd}) is crucial to device performance, an accurate determination of R_{sd} has been carried out [3]. Note that the R_{sd} value for strained devices is significantly reduced (~50%) by in-situ doping. Once R_{sd} is determined, the intrinsic $I_{d,lin}$ and $I_{d,sat}$ can be extracted by Eq. (1) and (2), respectively.

$$I_{d,lin}(int) = \frac{I_{d,lin}(ext)}{1 - I_{d,lin}(ext)(R_s + R_d)/V_d} \quad (1)$$

$$I_{d,sat}(int) = \frac{I_{d,sat}(ext)}{1 - I_{d,sat}(ext)R_s/V_{gst}} \quad (2)$$

3. Results & Discussion

Fig. 1 shows the intrinsic $I_{d,lin}$ and $I_{d,sat}$ enhancement of the strained devices. It can be seen that the intrinsic $I_{d,lin}$ and $I_{d,sat}$ are improved by about 100% and 50%, respectively. The enhancement in $I_{d,sat}$ is less than $I_{d,lin}$ because of velocity saturation. It indicates that the enhancement in saturation velocity (v_{sat}) for strained devices is smaller than the mobility (μ_{eff}) improvement. Since $E_{sat} = 2v_{sat}/\mu_{eff}$ [4], we can expect a smaller saturation electric field in strained devices. In other words, the saturation drain voltage (V_{dsat}) for the strained device should be smaller than its control counterpart for a given gate over-drive (V_{gst}). From the plot of R_{out} vs. V_d (Fig. 2), V_{dsat} can be extracted by linear extrapolation because R_{out} is proportional to (V_d - V_{dsat}) in the channel-length modulation region [5]. It can be seen from Fig. 2 that the strained PEFT indeed has a smaller V_{dsat} (~0.14V).

The impact of E_{sat} on g_m/I_d, an important figure of merit for analog performance, is mainly in the strong inversion regime. Fig. 3 shows g_m/I_d vs. L_{gate} at V_{gst} = 0.8V. The roll off of g_m/I_d as gate length decreases can be well modeled by the first term in Eq. (3). The lower g_m/I_d for strained devices can be attributed to the smaller E_{sat}.

$$\frac{g_m}{I_d} = \frac{\partial I_d/\partial V_g}{I_d} = \frac{1}{V_{gst}}\left(\frac{V_{gst} + 2E_{sat}L_{eff}}{V_{gst} + E_{sat}L_{eff}}\right) + \frac{(d\mu_{eff}/dV_g)}{\mu_{eff}} \quad (3)$$

Fig. 4 shows g_m/I_d vs. L_{gate} in the weak inversion regime (V_{gst} = 0.2V). It can be seen that g_m/I_d rolls up as gate length decreases. Moreover, the g_m/I_d for the strained device is significantly higher than its control counterpart, which can be attributed to the gate bias sensitivity of the mobility (the second term in Eq. (3)).

Fig. 5 shows the extracted mobility [3] vs. V_{gst}. It can be seen that μ_{eff} increases with V_g around V_{gst} = 0.2V. This is because in the low V_g region, the mobility is mainly determined by Coulombic scattering. The mobile carrier screening makes μ_{eff} increases with Q_{inv} (V_g). The larger slope for the strained device shown in Fig. 5 is responsible for the higher g_m/I_d observed in Fig. 4.

Fig. 6 shows R_{out} vs. V_d for various V_g. It can be seen that the R_{out} for strained devices is significantly reduced. The R_{out} in high V_d region is determined by drain induced barrier lowering and can be modeled by $1/(g_m \times dV_{th}/dV_d)$ [5]. The reduction in R_{out} for the strained device is mainly due to the enhanced g_m.

Fig. 8 compares the dc gain ($g_m \times R_{out}$) of the strained device with the control device. It can be seen that the dc gain for the strained device is slightly less than its control counterpart. This is because the strained device has a smaller R_{sd} and hence a higher V_d sensitivity of the threshold voltage, as verified by Fig. 7.

Fig. 9 shows the comparison of the gain-bandwidth product, which is defined as gain×g_m for a given capacitive load.

4. Conclusions

We have investigated the analog performance in uniaxial strained PMOS devices with sub-100 nm gate length. In the strong inversion regime, the g_m/I_d for strained devices is reduced due to decreased E_{sat}. In the weak inversion regime, nevertheless, the g_m/I_d for the strained device is significantly higher than the control device because of the higher V_g sensitivity of the mobility present in the strained device. This work may provide insights for analog design using advanced strained devices.

Acknowledgement

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References

[1] S.Takagi et al., *IEDM Tech. Dig.*, p.245, 2005.
[2] S. Thompson et al., *IEDM Tech. Dig.*, 2004.
[3] W. Chen et al., *VLSI-TSA Tech. Dig.*, p.143, 2006.
[4] Y. Cheng and C. Hu, "*MOSFET Modeling & BSIM3 User's Guide*," KAP 1999.
[5] J. H. Huang et al., *IEDM Tech. Dig.*, p.569, 1992.

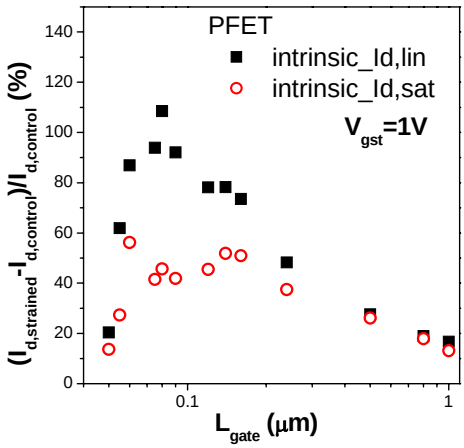

Fig.1 $I_{d,lin}$ and $I_{d,sat}$ enhancements for strained PFETs.

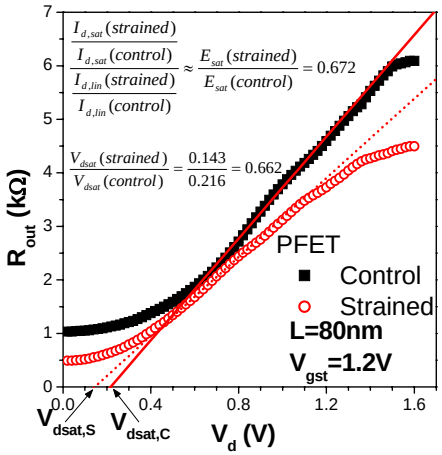

Fig.2 Output Resistance vs. V_d. The extracted V_{dsat} ratio corresponds to the E_{sat} ratio in the short channel device.

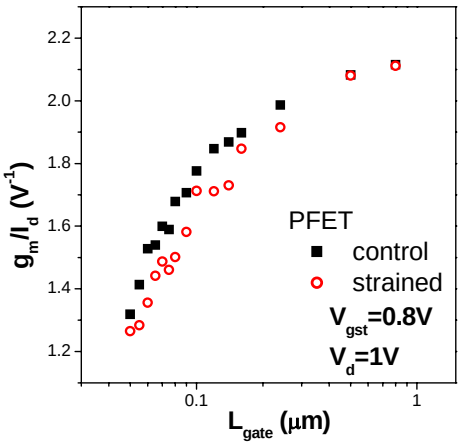

Fig.3 g_m/I_d at V_{gst}=0.8V vs. L_{gate}.

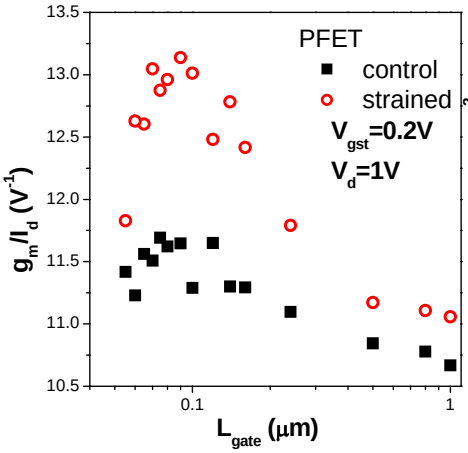

Fig.4 g_m/I_d at V_{gst}=0.2V vs. L_{gate}.

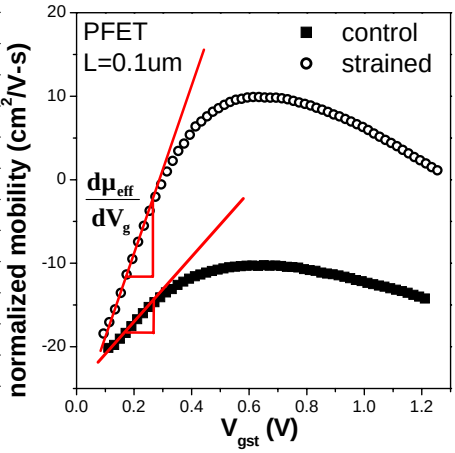

Fig.5 Extracted mobility vs. V_{gst}.

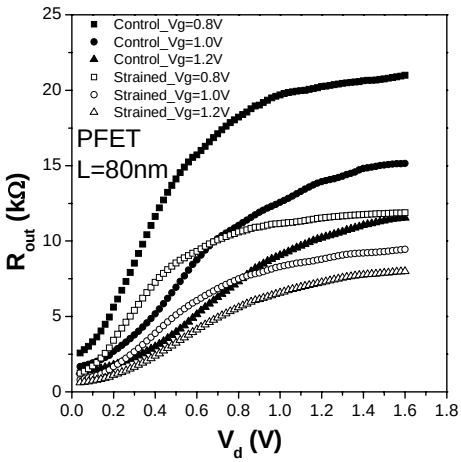

Fig.6 R_{out} vs. V_d for various V_g

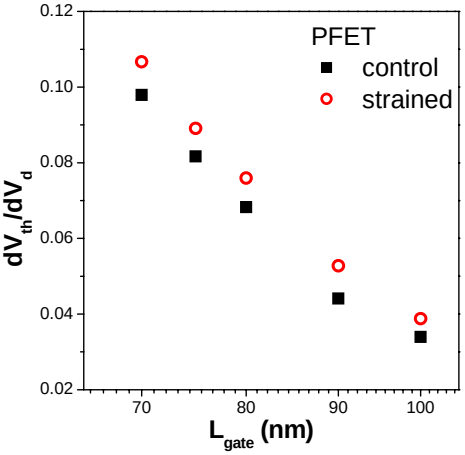

Fig.7 dV_{th}/dV_d vs. L_{gate}.

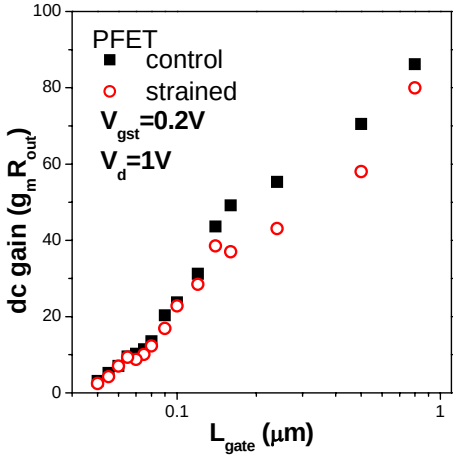

Fig.8 dc gain vs. L_{gate}.

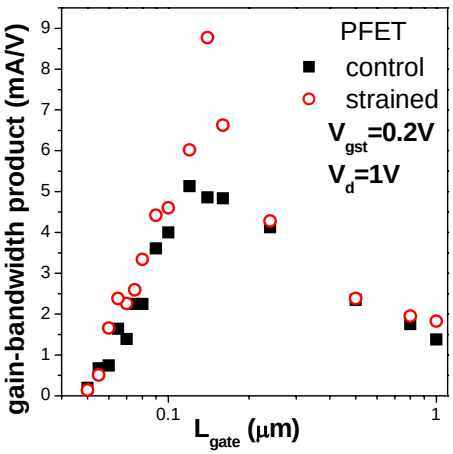

Fig.9 gain×bandwidth product vs. L_{gate}.