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Design of Cartesian Feedback Loop Linearization Chip for UHF band Using 0.6μm Bi-CMOS Technology

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1. Introduction

These days, digital communication systems such as TETRA are the main stream of LMR and public safety application. Unlike FM, TETRA system used π/4 DQPSK modulation. High frequency stability and power amplifier linearisation are main issues in digital modulation method. There are several methods such as feed forward, linear amplification with nonlinear device, Cartesian feedback loop (CFL) and adaptive predistortion in linearization. Among them, CFL method is the most available to LMR system due to feasible implementation [1].

In this paper, the linearization chip using Catesian feedback loop method is designed and fabricated. Espacially, because the phase shifter and forward attenuator are located in baseband region not in RF region, phase shifter and forward attenuator can be easily fabricated and detailed controlled.

2. The Operating Principle of Cartesian Feedback Loop

The effect of nonlinearity in feedback loop is analyzed with equivalent model of CFL in Fig.1 where the model represents only one of I or Q path.

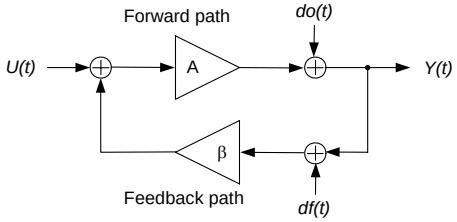

Fig.1. The Equivalent model of CFL Transmitter.

The distortion of forward loop is denoted *do(t)* which is generated in modulator and power amplifier, and the distortion of feedback loop is denoted *df(t)*, which is generated in demodulator. And open loop gain is denoted A , and feedback attenuation is denoted β. If the loop gain Aβ is assumed Aβ>>1, the output signal Y(t) is written as

$$Y(t) \approx \frac{U(t)}{\beta} + \frac{do(t)}{A\beta} - df(t) \qquad (1)$$

Equation (1) shows that loop Gain reduce non-linearity of forword path, feedback attenuation is total gain of CFL, and the nonlinearity of feedback path cannot be handled with CFL.

3. Cartesian Feedback Loop Chip Design

The forward path of designed Cartesian feedback loop chip is composed of conditional amplifier, image filter, error amplifier, I/Q modulator and DC-offset correction, variable attenuator for forward gain control, and phase shifter for phase control as in Fig. 2.

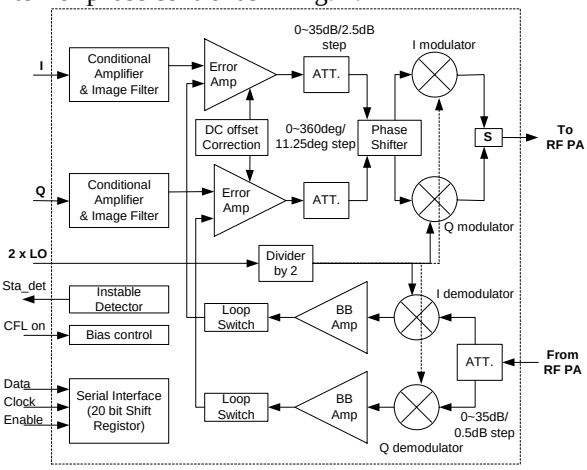

Fig.2. Block diagram of CFL chip

The magnitude of baseband I/Q signal is controlled with forward attenuator. The phase of signal is shifted with phase shifter, and the signal is modulated through forward path. The difference between distorted feedback signals and applied input signals are amplified through error amplifier. The error amplifier has an additional circuit to correct DC-offset at the input of modulator. The method of Sampling & hold is used. The circuit of phase shiter is shown in Fig.3. The phase shifter has two DACs. With two DACs and I/Q signals, the phase can be modified as Fig. 4 [2,3]. The gain of I/Q modulator is controlled by the ratio of Rs and R_L in Fig. 5.

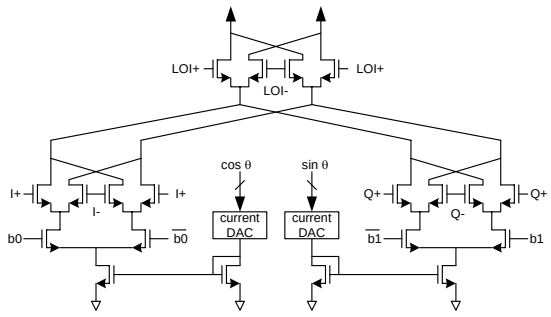

Fig. 3. The circuit of phase shifter

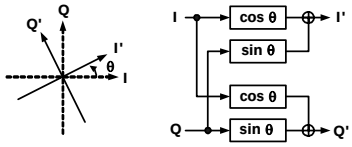

Fig. 4. Concept of phase shifting

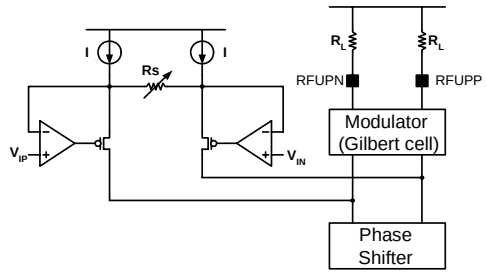

Fig. 5. The circuits of I/Q modulator for gain control

The feedback path of the designed Cartesian feedback loop is composed of variable attenuator for feedback gain control, I/Q demodulator, baseband amplifiers, and loop switches as in Fig. 2. A coupled signal of the output from the power amplifier is taken using an RF coupler which is external component of ASIC chip. The magnitude of RF signal is modified with feedback attenuator to keep linearity of I/Q demodulator and the signal is demodulated to baseband signals. Feedback attenuator is shown in fig.6. It is designed with two series inde-pendent attenuators to meet wide operating range. The I/Q demodulator is designed with Gilbert cell structure. For detailed control of total loop gain, the gain of baseband amplifer is controlled as 1dB range with 0.5dB step.

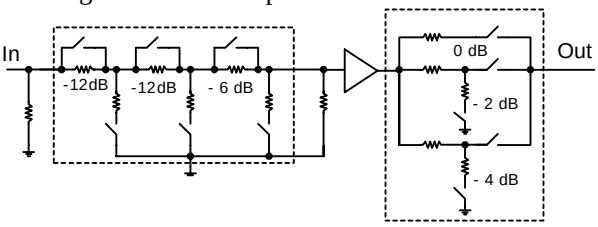

Fig. 6. The circuits of feedback variable attenuator

Besides forward path and feedback path, the I/Q generation block is designed with flip flop circuit when external local signal (760~1800MHz) is supplied. Bias control circuit and instable detector which can be detect the operation of CFL is in stable is designed.

The CFL is designed to cancel DC-offset and adjust amplitude & phase with external control signal which is interfaced with internal serial 20 bit shift registers.

4. Experimental Results

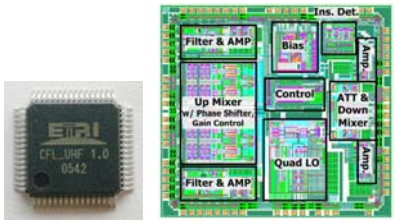

Fig. 7. The implemented Cartesian feedback loop chip

The size of implemented Cartesian feedback loop chip using 0.6μm BiCMOS technology based on Si is 3.77mm x 3.98 mm and the sizw of packaged chip (64pin TQFP) is 7mm x 7mm as in Fig. 7.

The characteristic of open-loop output and close-loop output is shown in Fig. 8 and Fig. 9. The external power amplifier module for 450MHz measurement was M68732HA of Mitsubishi, and 30dB directional coupler was used between CFL chip and power amplifier module. For 800MHz measurement, RA03M808M of Mutsubishi was used. From the test results, more than 30dBc of IMD level was improved and more than 25dBc suppression of carrier leakage was obtained at 33dBm (2W) of output power both 450MHz and 800MHz measurement. The test summary of the Cartesian feedback loop chip is shown in Table 1.

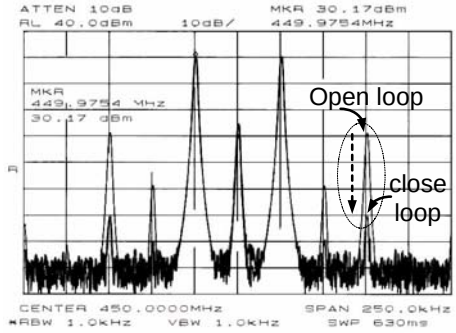

Fig. 8. Characteristic of CFL transmitter (@450MHz)

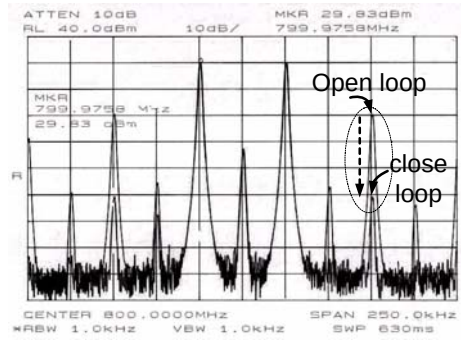

Fig. 9. Characteristic of CFL transmitter (@800MHz)

Table I The Summary of CFL chip Measurement

Item	Result
Operating Frequency	380 ~ 900MHz
Baseband Input Signal Amplitude	2V p-p (Max.)
Carrier Leakage	< -25dBc
IMD Level	< -30dB
Forward Gain Range & Steps	0 ~ 35dB & 2.5dB
Feedback Gain Range & Steps	0 ~ 35dB & 0.5dB
Phase Shifter Range & Steps	360° & 11.25°
LO Input Frequency	760~1800MHz

5. Conclusions

This paper describes the implemented Cartesian feedback loop chip using 0.6μm BiCMOS technology based on Si which is an essential device to improve transmitting power efficiency and miniaturization of mobile for LMR. More than 30dBc of IMD improvement and more than 25dBc carrier leakage suppression were acquired. Because forward gain and feedback gain can be controlled simultanously, the chip is suitable for the system which controls output power of mobile.

References

[1] A. Batman, et al, *Proc. 38th VTC* (1988)478.
[2] N. Sornin, et al, *RFIC Sym. Digest of papers* (2004) 145.
[3] M. Johansson et al, *Proc. 41th VTC* (1991) 439.