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A 77GHz T/R MMIC One-Chip Set Fabricated by a 0.15μm GaAs mHEMT Technology

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1. Introduction

Millimeter-wave automotive radar systems are a key technology for future adaptive cruise control systems. With an increased awareness and interest in safety issues on vehicular transportation, a variety of obstacle detectors has been researched and developed, among which a forward looking automotive radar has received special attention as it is considered to be an essential element to complete a vehicular safety system [1].

A promising way to meet the stringent cost requirements of these systems is the use of a monolithic microwave integrated circuit (MMIC) based on metamorphic high electron mobility transistor (mHEMT) technologies. In addition, the use of GaAs-based mHEMT results in higher circuit performance at even lower cost and a further reduction of chip size.

This paper describes the successful development of an MMIC one-chip set for automotive radar systems by using a 0.15 μm gate-length InGaAs/InAlAs/GaAs mHEMT technology on a GaAs substrate thinned to 100 μm [2], [3].

2. 0.15μm GaAs mHEMT Technology

In this paper, passivated 0.15 μm mHEMTs were fabricated by combining a wide head T-shaped gate using a dose split method of electron beam lithography and a highly selective recess etch process based on succinic acid. A double delta-doped mHEMT epitaxial structure on a GaAs substrate has been grown by molecular beam epitaxy (MBE). A cross-section of the mHEMT structure is shown in Fig. 1. The T-shaped gate for a 0.15 μm × 100 μm mHEMT device was sequentially formed using an E-beam lithography process followed by a selective wet etching of InGaAs over InAlAs using a succinic acid and H_2O_2 mixed solution and by a metal lift-off. The selective wet gate recess process using the succinic acid and H_2O_2 mixed solution showed an InGaAs etch rate of 120 nm/min and an etch selectivity of InGaAs to InAlAs layer of higher than 100.

The drain saturation current (I_{dss}) measured at V_{ds} = 2 V and V_{gs} = 0 V is 38 mA. The threshold voltage (V_{th}) is defined by a linear extrapolation of the square root of drain current versus gate voltage to zero current. V_{th} was measured as -0.9 V. The maximum g_m was measured as 700 mS/mm at V_{gs} = -0.5 V and V_{ds} = 2 V. The f_T and f_{max} of the devices were 130 and 230 GHz, respectively.

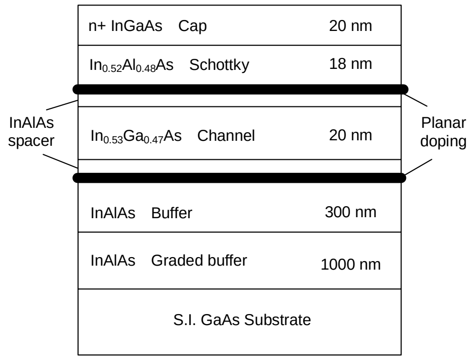

Fig. 1 Cross-section of double-doped mHEMT structure.

3. Experimental results

A. MMIC Transmitter

The MMIC transmitter consists of a frequency doubler, driver amplifier, a power amplifier and a lange coupler. In the frequency doubler, we designed an input circuit and output circuit to match at 38.25 GHz and 76.5 GHz, respectively. The operating conditions were near the pinch-off region so that high even harmonic power levels were generated. The external DC biasing conditions of V_d and V_g were 1.5 and –0.8 V, respectively, and the total current consumption was 10 mA.

The MMIC amplifiers were designed as single-ended 4-stage types. The first two stages used mHEMTs with 100 μm gate width and operated as class A amplifiers for gain consideration, while the last two stages employed 200 μm devices for power and efficiency requirements and operated at class A. The external DC biasing conditions of V_d and V_g were 2 V and –0.4 V, respectively, and the total current consumption of the MMIC PA was 150 mA. In the case of DA, the external DC biasing conditions of V_d and V_g were 2V and –0.6 V, respectively, and the total current consumption was 80 mA. The circuit simulation was accomplished by the use of the harmonic balance simulator with the HP root model for the active device.

The on-wafer measurement was performed using HP PNA N5250A 110 GHz network analyzer. The photograph of the fabricated MMIC transmitter is presented in Fig. 2. Fig. 3 shows the measured output power and conversion gain of the tramsmitter as a function of the input power level at 38.25 GHz. The transmitter achieved an output power of 11 dBm at 76.5 GHz with a conversion gain of 6 dB for an input power of 5 dBm and a 38.25 GHz input frequency. The transmitter also achieved a fundamental suppression of 32 dBc in a 76.5 GHz output frequency. The chip size was 5.1 mm × 2.2 mm.

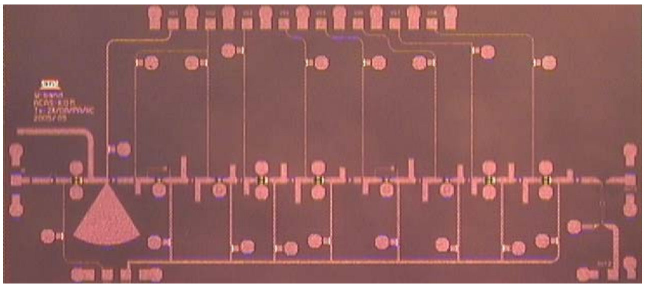

Fig. 2 Photogragh of the MMIC transmitter.

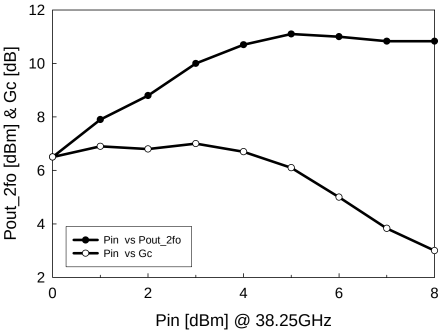

Fig. 3 Measured output power and conversion gain of the transmitter as a function of the input power level at 38.25 GHz.

8-stage Low Noise Amplifier

For the LNA, a 8-stage single-ended architecture using a common-source stage was chosen for the low noise figure and moderate gain with a MHEMT device of 2-finger 100 μm gate width. The gate width was chosen to minimize the complexity of matching circuits for a broadband operation and to prevent an excessive degradation of the amplifier's noise figure due to the loss in the matching circuits. To achieve a small chip size, short series microstrip elements were used along with shunt open stubs, which produced compact matching circuits. The LNA was also designed to operate at around a half of I_{dss}, rather than at the F_{min} bias condition to achieve a minimum noise figure. The external DC biasing conditions of V_d and V_g were 1 V and –0.8 V, respectively, and the current consumption of the first stage MHEMT was 7 mA. In the last seven stages, the external DC biasing conditions of V_d and V_g were 1.2 V and –0.5 V, respectively, and the total current consumption was 110 mA. The photograph of the fabricated LNA are presented in Fig. 4. The LNA achieved a gain of 35 dB in a band between 76 and 77 GHz with a noise figure of 5~6 dB. The chip size was 4.1 mm x 2.2 mm. The measurement results of the LNA are presented in Fig. 5.

4. Conclusions

This paper describes the successful development of an MMIC one-chip set for automotive radar sensor by using ETRI's 0.15 μm InGaAs/InAlAs/GaAs mHEMT technology on a 4-inch 100 μm thick GaAs substrate. The chip set consists of a transmitter and a 8-stage low noise amplifier. This MMIC one-chip set is suitable for 77 GHz automotive radar sensors and related applications in W-band.

References

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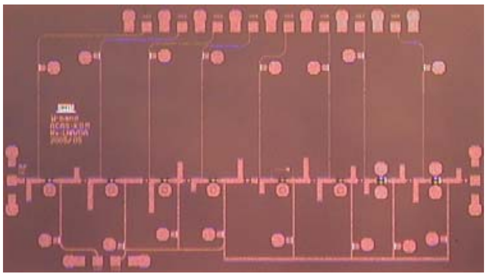
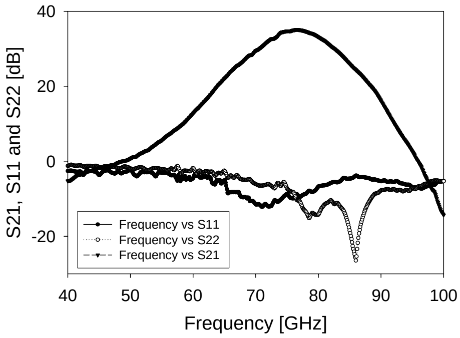
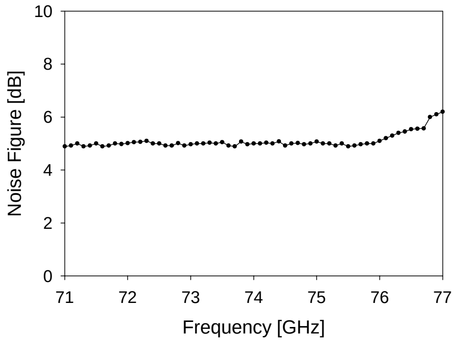


Fig. 4 Photogragh of the MMIC LNA.



(a) Small signal gain (S21), input return loss (S11), and output return loss (S22) as a function of frequency (40-100 GHz) for the fabricated MMIC LNA.



(b) Noise figure as a function of frequency (71-77 GHz) for the fabricated MMIC LNA.

Fig. 5 Measured results of MMIC LNA.