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Influence of T-gate shape on the device characteristics in SiN-assisted 0.12um AlGaAs/InGaAs PHEMT

Hokyun Ahn, Jong-Won Lim, Hong-Gu Ji, Woo-Jin Chang, Jae-Kyoung Mun and Haecheon Kim

RF Circuit Group, IT Convergence and Components Laboratory, Electronics and Telecommunications Research Institute, Daejeon 305-350, Korea
Phone: +82-42-860-6135 E-mail: hkahn@etri.re.kr

1. Introduction

Recently, millimeter wave applications such as high speed wireless communications, collision avoidance car radar systems and millimeter wave video transmission systems have been developed. Especially, unlicensed 60GHz-bands are of growing interest for high rate personal area network (WPAN) (IEEE 802. 15. 3) and high rate wireless local area network (WLAN) [1]. Millimeter wave MMICs of such applications have been fabricated through III-V compound-based technology related to active devices such as GaAs-based HEMT, InP-based HEMT and InP-based HBT. Especially, p-HEMT devices are widely utilized as active devices of millimeter wave MMICs due to an excellent and stable RF performance. The gate shape of the p-HEMT device is correlated to parasitic capacitances including C_{gs} which have effects on RF performances including a cut-off frequency (f_T) and a maximum frequency of oscillation (f_{max}) [2]. In this work, we describe the fabrication technology of SiN-assisted 0.12um double deck T-gate AlGaAs/InGaAs p-HEMT. This paper also presents the effect of the gate head size on the DC and RF characteristics of SiN-assisted 0.12um double deck T-gate AlGaAs/InGaAs p-HEMT devices and the device performance of the p-HEMT at 0.4um of the gate head size

2. Experiments

The double planar doped AlGaAs/InGaAs p-HEMT structures on 4-inch semi-insulating GaAs substrates were grown by molecular beam epitaxy. The p-HEMT structures consist of a 500nm thick GaAs buffer layer grown on the GaAs substrate, 30 layers of $Al_{0.23}Ga_{0.77}As$-GaAs superlattices, a 50nm thick $Al_{0.23}Ga_{0.77}As$ buffer layer, a bottom planar Si doped layer (bottom : 1.0 x 10^{12} cm^{-2}), a 2nm thick bottom $Al_{0.23}Ga_{0.77}As$ spacer, a 12nm thick $In_{0.2}Ga_{0.8}As$ channel layer, a 3.5nm thick top $Al_{0.23}Ga_{0.77}As$ spacer, a top planar Si doped layer (top : 4.5 x 10^{12} cm^{-2}), a 25nm thick undoped $Al_{0.23}Ga_{0.77}As$ schottky layer and a 40nm undoped GaAs cap layer. 0.12um GaAs p-HEMT devices were fabricated by a silicon nitride assisted double deck T-gate process. After a mesa isolation, ohmic contacts were formed by thermal evaporation of AuGe/Ni/Au and then alloyed by a rapid thermal annealing. A drain-to-source distance of these ohmic contacts with a gate-to-source distance of 1um was 2.5um. For the purpose of surface passivation, a 500Å thick silicon nitride layer was deposited by a plasma-enhanced chemical vapor deposition (PECVD). T-gate patterning was performed by an e-beam lithography process. 950 PMMA was used as the resist of gate foot patterning. After the patterning, the silicon nitride layer was etched by a reactive ion etching (RIE) process using an Oxford Plasma Technology Plasmalab System 100. PMMA/P(MMA-MAA)/PMMA tri-layer resist system was used to form T-shaped gate pattern. After these resists were exposed by Leica EBPG 5000 plus system with 100kV acceleration voltage, the tri-resists were developed by mixed solutions of MIBK and IPA. The critical dimension size of the 1st-deck head patterns varied from 0.20um to 0.39um. The critical dimension size of the 2nd-deck head patterns varied from 0.4um to 1.0um in order to investigate the variation of device characteristics with the change of the gate head size. The height of the gate head was fixed at 2500Å. After patterning, a gate recess process was performed by an electron cycrotron resonance (ECR) etching process and a wet chemical etching process in H_3PO_4:H_2O_2:H_2O = 4:1:180 solution. Ti/Pt/Au (0.6um) layers were deposited and lifted-off. Fig. 1 shows a cross-section SEM image of SiN-assisted T-shape gate electrode with 0.12um gate length. DC and RF characteristics of the p-HEMT device were measured by HP 4155B and HP8510C network analyzer, respectively.

3. Results

DC and RF performances of AlGaAs/InGaAs p-HEMT with 0.12um gate length and a total gate width of 100um were investigated at different gate head sizes. The device having a good RF performance such as a high cut-off frequency requires a high transconductance and a low C_{gs} value. Fig. 2 shows that the optimum 1st-deck head size was 0.22um. Table 1. shows that the maximum extrinsic transconductance (g_m) at 1.5V of drain voltage and the cut-off frequency (f_T) decreased with the gate head size. C_{gs} value increased with the gate head size. (Fig. 3) Therefore, the device with 0.4um of gate head size shows the best performance among three conditions of gate head sizes. (Fig. 3) This result suggested that a capacitance between the gate head metal and the channel layer of the p-HEMT device has an effect on the whole gate to source parasitic capacitance (C_{gs}) and the RF performances including cut-off frequency [2]. At 0.4um of gate head size, DC and RF characteristics of the p-HEMT device with two finger gates of 0.12um length x 50um width were measured as follows. Fig. 4 shows drain current as a function of source-to-drain voltage (V_{ds}) for the 0.12um p-HEMT

devices fabricated by the SiN-assisted gate process. As shown in Fig. 4, the p-HEMT devices exhibited a good pinch-off characteristics at a drain voltage of 1.5V and a gate voltage of -1.2V. The drain saturation current (I_{dss}), measured at V_{ds} = 1.5V and V_{gs} = 0V, was 12.2mA for 50um of total gate width. The extrinsic transconductance and the drain current as a function of source-to-gate voltage were measured at source-to-drain (V_{ds}) of 1.5V, as shown in Fig. 5. The threshold voltage, measured at V_{ds} = 1.5V, was -1.12V. The maximum transconductance (g_m) and the drain current at 1.5V of drain voltage and 0.4V of gate voltage were 511mS/mm and 20.6mA, respectively. The S-parameters for the p-HEMT device were measured from 0 to 50GHz. The cut-off frequency (f_T) was obtained by extrapolating the current gain, H_{21}, to unity with the slope of -20dB/decade, and the maximum frequency of oscillation (f_{max}) was extracted by parallel shifting of -20dB/decade slope line to MSG/MAG plot. The cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}), measured at V_{ds} = 1.5V, were 97GHz and 193GHz, respectively.

4. Conclusions

In this paper, the fabrication technology of the SiN-assisted 0.12um double deck T-gate was described. This paper also presents the effect of the gate head size on the DC and RF characteristics of SiN-assisted 0.12um T-gate AlGaAs/InGaAs p-HEMT devices.

References

[1] K. Ohata, K. Maruhashi, M. Ito, S. Kishimoto, K. Ikuina, T. Hashiguchi, K. Ikeda and N. Takahashi, IEEE MTT-S Dig. (2003) 373.

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Table I Device characteristics as a function of the 2nd-deck head size for the 0.12um p-HEMT devices.

Head Size	V_{th} (V)	Peak g_m (mS/mm)	I_{ds} (mA)	f_T (GHz)	f_{max} (GHz)	C_{gs} (pF)
1.0um	-1.16	497	20.49	90.94	184.05	0.074
0.5um	-1.27	501	19.86	95.20	190.26	0.071
0.4um	-1.12	511	20.62	96.80	192.62	0.071

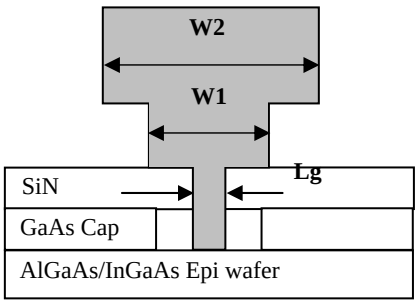

Fig. 1 Cross-section SEM image of SiN-assisted p-HEMT. (W1 : 1st-deck head size, W2 : 2nd-deck head size, Lg : gate foot size)

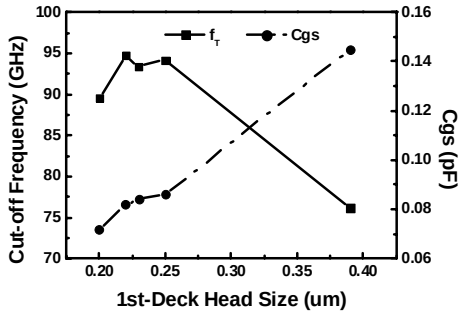

Fig. 2 Variation of Cut-off frequency and gate-to-source parasitic capacitance (C_{gs}) with the change of the 1st-deck head size.

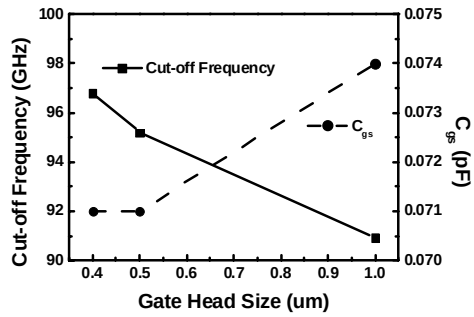

Fig. 3 Variation of Cut-off frequency and gate-to-source parasitic capacitance (C_{gs}) with the change of the 2nd-deck head size.

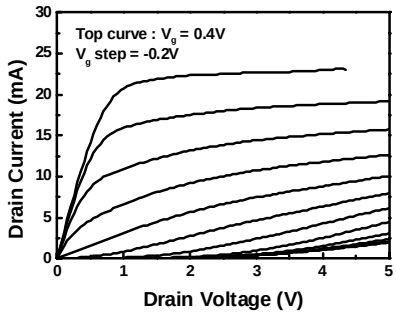

Fig. 4 Drain current as a function of source-to-drain voltage (V_{ds}) for the 0.12um p-HEMT devices with 0.4um of gate head size.

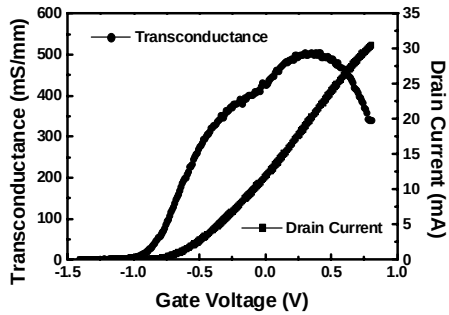

Fig. 5 The extrinsic transconductance and drain current at V_{ds} = 1.5V as a function of source-to-gate voltage for the 0.12um p-HEMT devices with 0.4um of gate head size.