Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 620-621

P-6-5

Pt Buried Gate E-pHEMT with High $V_{G.ON}$ and Reduced Surface Trap Effects

Kyoungchul Jang[1], Gyungseon Seol[1], Sungwon Kim[1], Jincherl Her[1], Jaehak Lee[2], Kwangseok Seo[1]

[1]Seoul National Univ., School Of Electrical Engineering and Computer Science
San 56-1, Shillim-dong, Kwanak-ku, Seoul 151-744, Korea
Phone: +82-2-877-0298 E-mail: liberty@snu.ac.kr
[2]Theleds Co., LTD.
393-13 Jwahang-ri, Wonsam-myeon, Cheoin-gu, Yongin-si, Gyeonggi-do 449-871, Korea

1. Introduction

Enhancement-mode pseudomorphic High Electron Mobility Transistor (E-pHEMT) is in severe competition with Hetero-junction Bipolar Transistor (HBT) for handset PA market. E-pHEMT has a merit of single power supply system over depletion-mode pseudomorphic HEMT (D-pHEMT). But it has a demerit of small drain current density due to the narrow gate voltage swing range from threshold voltage (V_{TH}) to gate forward turn-on voltage ($V_{G.ON}$). There have been many researches to obtain high $V_{G.ON}$ for larger gate swing range [1] [2]. In our prior research we showed that surface trap density in the side recess region can be a limiting factor for the increase of the drain current density of E-pHEMT with high $V_{G.ON}$ and proposed 0.5 μm gate $In_{0.49}GaP/Al_{0.45}GaAs$ barrier E-pHEMT with the drain current density of 450 mA/mm at the V_{GS} of 1.5 V [3].

It is necessary to reduce source resistance (R_S) for the fabrication of E-pHEMT with higher current density. We found that the resistance of gate side recess region (R_{SIDE}) took up a large portion of R_S. Pt buried gate process was often used for the fabrication of InGaAs/InAlAs E-pHEMTs [4]. The Pt buried gate InGaAs/InAlAs E-HEMT with the barrier thickness of depletion-mode HEMT showed a lower R_S than the E-HEMT fabricated in a conventional manner [4]. However Pt buried gate E-HEMTs tend to have low $V_{G.ON}$ of depletion-mode HEMTs. In this paper we propose the Pt buried gate E-pHEMT with high $V_{G.ON}$ and reduced surface trap effects in gate side recess region.

2. Source Resistance

The E-pHEMT of our previous research [3] had the R_S of 1 Ω.mm which is much higher than that of conventional HEMTs. The R_S of HEMT is composed of the ohmic contact resistance (R_C), the resistance due to the sheet resistance of a layer structure (R_{SHEET}) and R_{SIDE}. We performed a Transmission Line Method (TLM) measurement to measure the real R_C to channel layer after removing some of the cap layer between drain and source electrodes. The R_C to channel layer was 0.35 Ω.mm while the R_C measured in conventional TLM was 0.15 Ω.mm. The R_{SHEET}, which could be easily calculated from the sheet resistance of the epitaxial layer and layout parameter, was 0.1 Ω.mm. The R_{SIDE} was 0.55 Ω.mm which took up around 50 % of R_S. Thus reducing R_{SIDE} was essential for the fabrication of E-pHEMT with high current density.

3. Layer Structure and Fabrication

Figure 1 shows the E/D-mode pHEMT layer structure designed for this study. Basically $Al_{0.22}GaAs$ and $In_{0.22}GaAs$ were used for barrier and channel layer. As we wanted fairly high $V_{G.ON}$ for E-mode HEMT, wide band-gap material of $Al_{0.45}GaAs$ was inserted into the E-mode barrier. $In_{0.49}Gap$ etch stop layer not only offers excellent etch selectivity but also causes less deep level defects. [3] A thin N+ doped GaAs was used as a D-mode barrier. Only when this layer has proper thickness and doping density, fabricated Pt buried gate HEMT could have a high $V_{G.ON}$ and reduced surface trap effects in the side recess region simultaneously. InGaP etch stop layer was inserted for D-mode HEMT fabrication. Finally highly N+ doped GaAs layer was used as cap for good ohmic contact.

Mesa isolation was done using wet etching. Ohmic metal of Ni/Ge/Au/Ni/Ag/Au was evaporated and annealed at 470 °C. 0.5 μm gates were defined and phosphoric acid etchant (H_2PO_4:H_2O_2:H_2O=1:1:25) was used for the removal of GaAs layer. Gate recess was done for 20s for the fabrication of D-mode pHEMT. Pt/Ti/Pt/Au was evaporated as a gate metal. Pt annealing was done using rapid thermal annealing (RTA) in N_2 ambient. After Pt annealing process $In_{0.49}GaP$ etch stop layer in the side recess region was removed using the mixture of H_2PO_4:HCl=1:1. Devices were fully passivated using 1000 Å thick Si_3N_4 in remote plasma enhanced chemical vapor deposition (RPECVD).

4. Measurement

Figure 2 shows the transfer curves of the device for various Pt annealing temperature. After the annealing it had the positive V_{TH}, the gm.max of 470mS/mm, the low $V_{G.ON}$ of 0.7 V and a high reverse leakage current level before InGaP layer removal. Figure 3 shows the gate I-V curves of the E-pHEMT before and after InGaP layer removal in the side recess region. The E-pHEMT showed a higher $V_{G.ON}$ of 1.0 V after InGaP layer removal. The removal of InGaP layer induced the surface depletion in the side recess region that blocked the gate current path near the cap to barrier interface without harming the flow of drain current.

Figure 4 shows the transfer curves of the E-pHEMTs fabricated in the Pt buried gate process and the conventional etch stop gate process. The Pt buried gate E-

pHEMT had the $g_{m.max}$ of 470 mS/mm and the R_S of 0.9 Ω.mm while the etch stop gate E-pHEMT had the gm.max of 370 mS/mm and the R_S of 1.4 Ω.mm. The R_S differences of these two devices are due to the reduced surface trap effects in the side recess region.

5. Conclusions

The gate side recess region of E-pHEMT induced a high resistance to R_S. Pt buried gate process, which is a way to reduce the R_S of E-pHEMT, reduced the $V_{G.ON}$ of E-pHEMT. The current flow paths of gate current and drain current are not identical. A good portion of gate current flows along the cap to barrier interface, while most of drain current flows in the channel layer. By inducing proper amount of surface depletion to the Pt buried gate E-pHEMT, the gate current could be reduced without the deterioration of the drain current.

Acknowledgements

This work was financially supported by the National program for Tera-Hz Level Integrated Circuits of the Minister of Science and Technology as one of the 21st Century Frontier program

References

[1] E. Glass et al, IEEE MTT-S Dig. pp. 1399-1402 (19 97).

[2] Y. Bito, T. Kato, T. Kato and N. Iwata, IEEE GaAs Dig. pp. 255-258 (2000).

[3] K. Jang, J. Lee, J. Lee and K. Seo, JJAP **45** 4B (2006) 3355

[4] K. J. Chen, T. Enoki, K. Maezawa, K. Arai and M. Yamamoto, IEEE Trans. ED **43** 2 (1996) 252

Layer	Material
Cap	n+ GaAs
D mode barrier	$In_{0.49}GaP$
	n+ G aAs
E mode barrier	$In^{0.49}GaP$
	$Al_{0.45}GaAs$
	$Al_{0.22}GaAs$
	Si delta doping
	$Al_{0.22}GaAs$
Channel	$In_{0.22}GaAs$
Barrier	$Al_{0.22}GaAs$
	Si delta doping
	$Al_{0.22}GaAs$
Buffer & Substrate	

Fig. 1 Layer structure for E/D HEMT

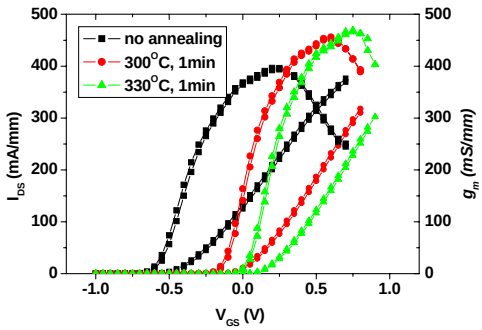

Fig. 2 Pt annealing temperature dependence of the transfer curves of the fabricated device

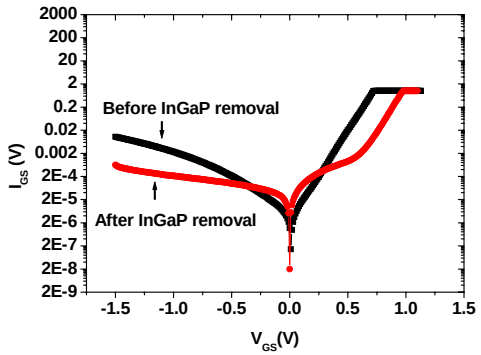

Fig. 3 Gate I-V curves of the E-pHEMT before and after InGaP removal in the gate side recess region.

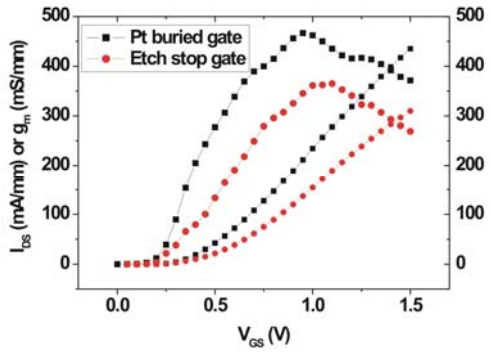

Fig. 4 Transfer curves of the Pt buried gate E-pHEMT and the etch stop gate E-pHEMT.