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P-6-6

Direct Calculation of Source Parasitic Resistance in AlGaAs/GaAs HEMTs

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1. Introduction

The performance of field-effect transistors (FETs) is significantly influenced by the parasitic series resistance between the gate and the source contact. The source series resistance is known to degrade both transconductance and noise figure of FET devices. In addition, the source resistance increases on-resistance of an FET, leading to inferior drain efficiency of the power FET as well as increased insertion loss of the switching FET. The experimental determination of the source resistance has been discussed in many publications, where the so-called end-resistance is the most generally-accepted measurable value as a source resistance [1,2]. However, no theoretical studies have been made concerning the true source resistance affecting the bias dependent transconductance characteristics of an FET.

In this paper, parasitic series resistances in AlGaAs/GaAs HEMTs were directly evaluated using an ensemble Monte Carlo simulation. Simulation results indicate that the source series resistance is principally governed by the component R_1 (series resistance between the source contact and the gate) and becomes also dominated by the component R_{ch} (channel resistance under the gate) when the device has a high source resistance of more than 1Ωmm.

2. Simulation

Figure 1 shows the schematic cross-section of an AlGaAs/GaAs HEMT used in our simulation. The device consists of an undoped GaAs channel layer with a thickness of 90nm and an n-type AlGaAs barrier layer with a donor concentration of 3×10^{18}cm^{-3}. The buried gate recess structure was assumed with a gate length of 0.5μm. The thickness of n-AlGaAs under the gate was chosen to be 30nm so that the device has a threshold voltage of around -2V. In order to evaluate the dependence of transconductance on the source resistance, the distance between source and gate (L_{sg}) was varied from 300 to 2500nm, while the distance in the drain side (L_{gd}) was fixed to be 1500nm. Dynamics of carrier transport in the device was simulated based on an ensemble Monte Carlo algorithm coupled with a self-consistent 2D Poisson equation[3]. The simulator incorporates an analytical 3-valley band structure and considers polar optical phonon scattering, intervalley phonon scattering and ionized impurity scattering. The effects of 2D electronic states at the heterojunction interface were not taken into account.

3. Results and Discussion

Figure 2 shows an example of electrostatic potential, evaluated along the GaAs channel, plotted as a function of the distance from the source contact. From the linear dependence between A and B, the series resistance (R_1) between source and gate is defined by the voltage difference (V_1) divided by the source current (I_s). Similar dependence was observed between C and D, and the voltage drop (V_2) was extracted between gate and drain. The channel resistance (R_{ch}) is thus determined by defining the channel voltage (V_{ch}) as V_{ds}-V_1-V_2. In this work, the end resistance (R_{end}) was defined by the following equation [2].

$$R_{end} = R_1 + R_{ch} / 2 \qquad (1)$$

Figure 3 shows the calculated R_1 and R_{end} as a function of the drain voltage. When the drain voltage is very low in the linear region, the difference between R_1 and R_{end} is negligible. As the drain voltage is increased into the saturation region, the channel voltage under the gate increases and thus R_{end} increases linearly, while R_1 remains constant irrelevant to the drain voltage. Figure 4 shows R_1 and R_{end} as a function of the gate voltage. When the gate is positively biased to give rather large drain current, there is negligible difference between R_1 and R_{end}. As the gate voltage is decreased toward pinch-off, R_{end} exhibits a sudden increase, while R_1 is kept constant. Figure 5 shows R_1 and R_{end} as a function of the distance between source and gate (L_{sg}). With the increase in L_{sg}, R_1 increases linearly while R_{end} exhibits rather flat dependence, reflecting the gate bias dependence of R_{end}, as shown in Fig.4.

Figure 6 shows the transconductance, estimated under the constant drain current of 200mA/mm, as a function of the source resistance defined by R_1 or R_{end}. Also plotted is the well-known analytical formula, describing the relation between the extrinsic transconductance and the source resistance. Here, an intrinsic transconductance of 280mS/mm was assumed. It was found that the extrinsic transconductance is determined by R_1 in the small source resistance region, while it becomes more dominated by R_{end} in the high source resistance region. Since the experimental R_{end} is estimated under forward gate bias conditions, the difference between R_1 and R_{end} is relatively small, as shown in Fig.4. Therefore, it was verified that the experimentally determined R_{end} reasonably describes the dependence of transconductance on the source resistance of HEMTs.

4. Conclusions

Parasitic series resistances in AlGaAs/GaAs HEMTs were directly evaluated using an ensemble Monte Carlo simulation. It was found that the source series resistance is principally governed by the series resistance between

source and gate. The plot of simulated transconductances under an identical drain current indicated that the experimentally measured R_{end} is a reasonable approximation as a true source resistance that determines extrinsic transconductance characteristics.

References

[1] K.W. Lee et al., IEEE Trans. Electron Devices, Vol. ED-31, pp.1394-1398 (1984).

[2] K. Lee et al., IEEE Electron Device Lett., Vol. EDL-5, pp.5-7 (1984).

[3] I. C. Kizililyalli et al., IEEE Trans. Electron Devices, Vol.38, pp.197-206 (1996).

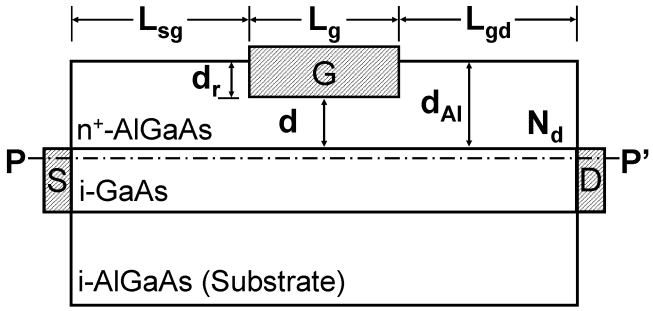

Fig.1 Schematic cross-section of AlGaAs/GaAs HEMT.

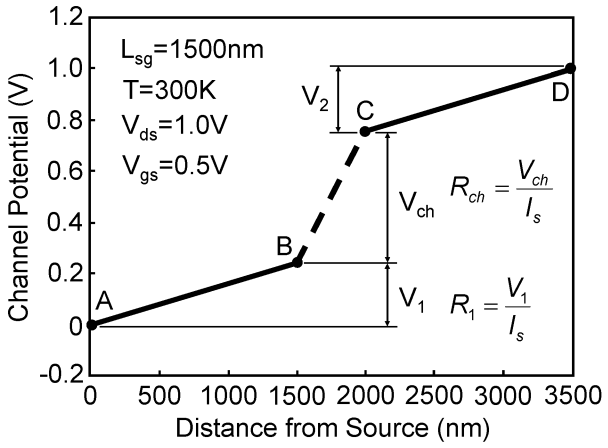

Fig.2 Potential distribution along channel.

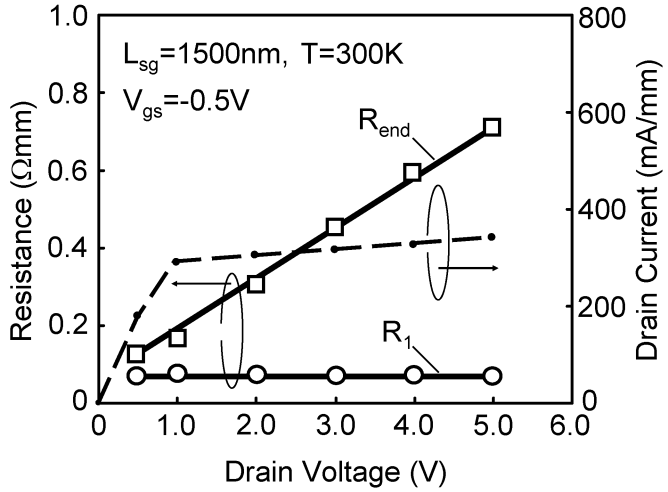

Fig.3 Calculated R_1 and R_{end} as a function of drain voltage.

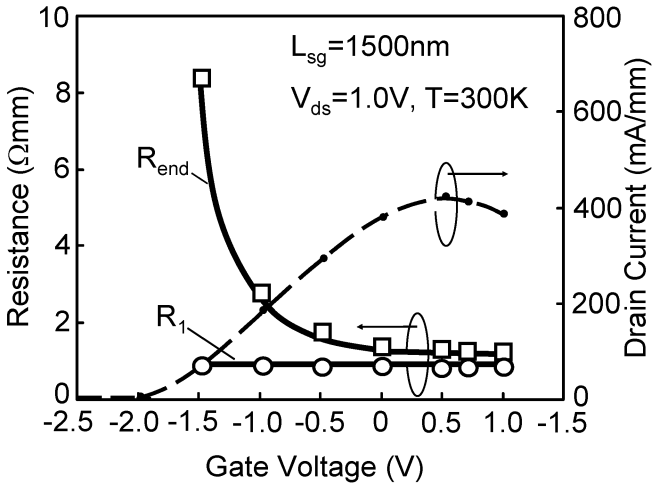

Fig.4 R_1 and R_{end} as a function of gate voltage.

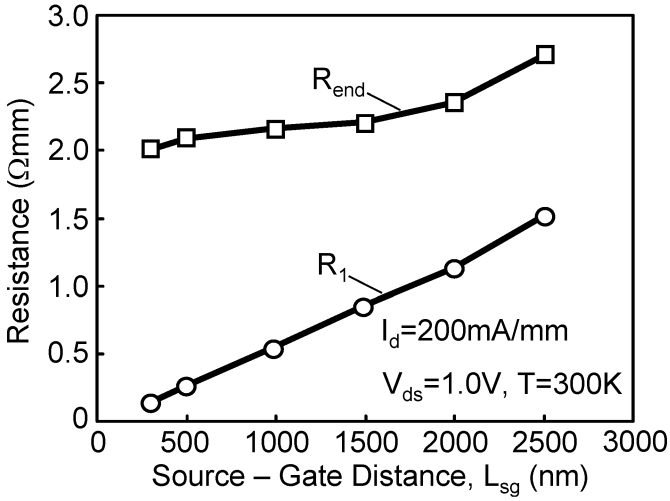

Fig.5 R_1 and R_{end} as a function of distance between source and gate.

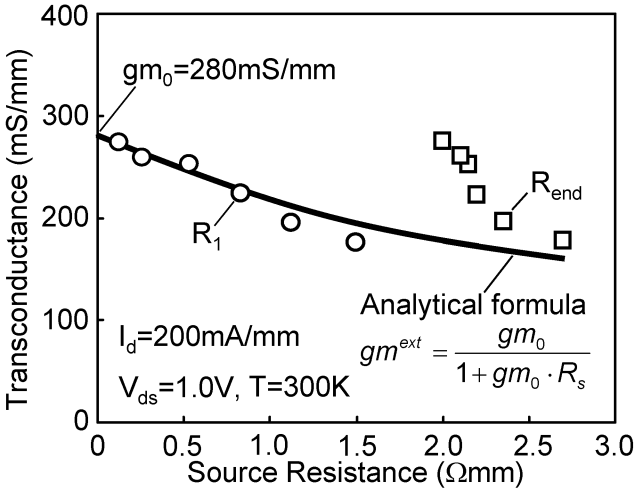

Fig.6 Transconductance as a function of source resistance. Drain current is fixed at 200mA/mm. Solid line is calculated by analytical formula assuming gm_0 of 280mS/mm.