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A Novel Method for the Preparation of Si Nanowires

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1. Introduction

Si nanowire (SiNW) structures have recently attracted a lot of attentions. By taking advantage of the high surface-to-volume ratio inherent in the structure, NWs can provide high surface sensitivity for sensing device applications [1], [2]. The preparation methods of NWs could be categorized into two types, namely, top-down and bottom-up [3]. Among a number of bottom-up approaches, catalytic growth is probably the most popular. This method is suitable for preparing various kinds of NW materials and can even be applied for forming NW heterostructures [4]. It is thus very flexible and suitable for the feasibility study in laboratories. However, there also exist some issues, such as the difficulty in controlling the NW dimensions including length and diameter, as well as the NW orientation [5]. Moreover, the use of metal nano particles as the catalyst represents a potential contamination issue. These issues may hinder practical applications. Besides, the manufacturing of NW devices may suffer from the uncontrollability of structural parameters such as NW's length and diameter. Thus the precise positioning of the NWs represents another major obstacle for reliable device fabrication. These issues probably could be overcome by using the top-down approaches that usually rely on advanced lithography tools, like the DUV steppers and e-beam lithography technique [6], to form the NW structures. Nevertheless, the process cost could be high owing to the use of costly lithography tools.

In this work we proposed and demonstrated a simple and promising approach that could effectively address the above issues. This approach belongs to the top-down category albeit no costly lithography step is involved.

2. Preparation and Characterization of SiNWs

Detailed process sequence is illustrated in Fig. 1. Firstly, the starting Si wafers were oxidized, then a g-line stepper was used to form periodic PR patterns on the surface. The PR patterns were transferred to the underlying oxide layer by a plasma etch step. Oxide trimming was subsequently performed in an HF solution to further shrink the dimension of the oxide structure. This step allows us to scale the patterns into nano-scale dimension without resorting to expensive equipments. With careful tuning of the etching conditions, the precise control over the structural dimensions is feasible. After the oxide trimming, the PR patterns were stripped off, followed by a Si etch step performed in a high-density plasma etcher with the remaining oxide structures as the hardmask.

Figure 2 shows several Si pillar structures having a height of around 2 μm. Figure 2(a) shows a sample that did not receive the oxide trimming treatment and the diameter is 1.3 μm. Figure 2(b)~(d) are the formed NW structures with diameter of 40, 30, and <30 nm, respectively. Note that the structure becomes very flexible when scaled below 30 nm.

Using the above samples, we've also developed a method to prepare a solution that contains Si NWs, as shown in Fig. 3. Wafers were then immersed in the solution and treated with megasonic oscillation to break the NWs from their root. Afterwards, wafers were removed and the solution was harvested. The solution could then be used as a source for forming aligned Si NWs on many kinds of substrates for electronic applications [7], [8].

Figure 4 shows the TEM image and the corresponding diffraction pattern of a SiNW structure. It is seen that good crystallinity could be retained.

3. Conclusion

In conclusion, we have proposed and demonstrated a very simple and low-cost method to fabricate silicon nano wires without resorting to expensive tools or complex processes. Besides, the processed wafers could be recycled and reused after suitable treatment. In contrast to the conventional approach using metal catalytic growth, the new method is essentially metal free and provides good control over the NW length, diameter, and orientation.

Acknowledgments

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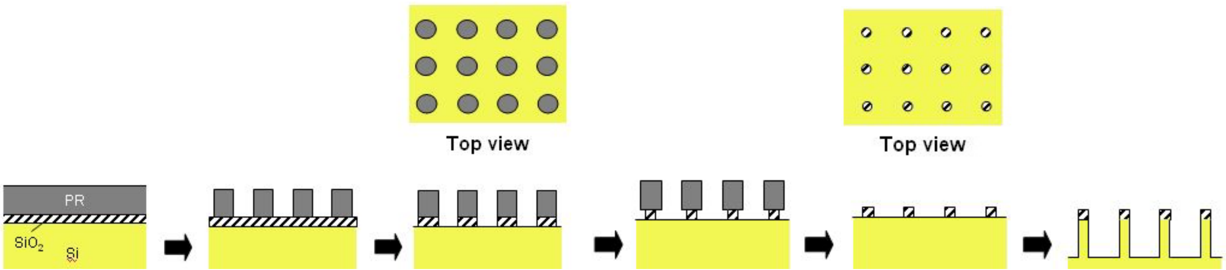

Fig.1 Process flow for the preparation of SiNWs.

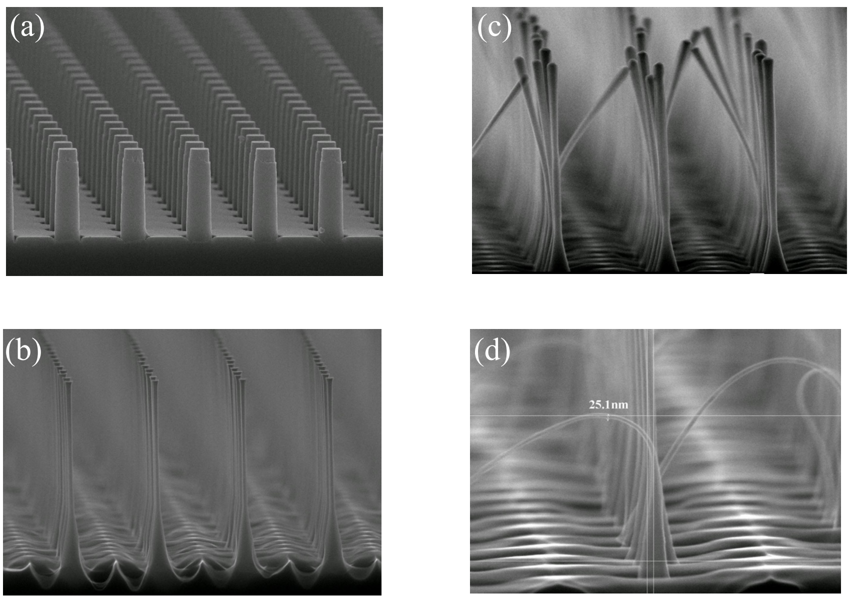

Fig.2 SEM pictures of the patterned Si pillar structures with diameter (a) 1.3 μm, (b) 40 nm, (c) 30 nm, and (d) <30 nm.

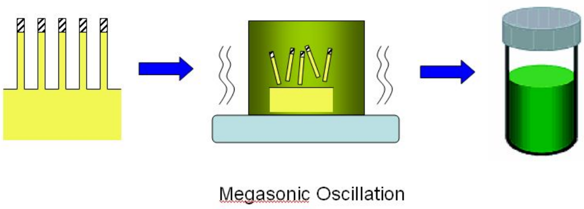

Fig.3 Preparation of NW solution.

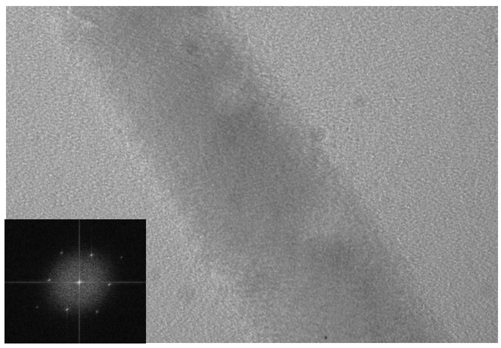

Fig.4 TEM image of the SiNW.