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Growth of III-V epitaxial material on Si Substrates for high-speed electronic applications

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1. Introduction

The heteroepitaxial growth of GaAs on Si substrates has attracted great attention in recent years due to the potential integration of the Si and GaAs based devices. GaAs has advantages over Si for some application due to higher electron mobility, wider bandgap, and direct bandgap. Silicon, however, has several advantages over GaAs such as larger area, less brittle substrates, and higher thermal conductivity. The main problems to overcome on growing GaAs on Si by heteroepitaxy are the large lattice mismatch of 4% and the difference in the thermal expansion coefficients (63%) of these two materials.[1] To achieve high quality device structure, it is necessary to reduce the dislocations density in the epitaxial layer.

In this work, we use two stage SiGe buffer layer structure with a top Ge layer.[2] Because The lattice constant and thermal expansion coefficient of Ge are almost identical as GaAs. Using two stage Ge/SiGe as buffer can solve the mismatch problems of the interface between GaAs and Si.

2. Experimental

The growth of the SiGe and Ge buffer layers was carried out using an urta-high vacuum chemical vapor deposition (UHV/CVD) system with a base pressure of less than 2×10^{-8} torr. First, a 4-inch Si wafer 6^0 off (100) toward <110> direction was cleaned by 10% HF dipping and high-temperature baking at 800 ^oC in the growth chamber for 5 min. Then, a 0.8 μm $Si_{0.1}Ge_{0.9}$, a 0.8 μm $Si_{0.05}Ge_{0.95}$, and a 1.0 μm Ge layer were grown at 400 ^oC in sequence. Between successive layers, growth was interrupted for an in situ 15 min 750 ^oC annealing. After Ge layer were grown on Si substrate, the sample was switched to the MOVPE system to grown GaAs on the Ge/SiGe/Si heterostructure at 40 Torr reactor pressure. Low temperature (LT) GaAs buffer with 100nm was grown at 430 ^oC first. Then an undoped 1.0 μm GaAs layer was grown at 630 ^oC. The 15 pairs AlGaAs/GaAs superlattices were grown to restrict the dislocation propagation and modify the surface, GaAs MESFET structure with 3.0 μm undoped GaAs layer, a 1500 Å channel doped at 5×10^{17} cm^{-3} and a 500 Å contact layer doped at 5×10^{18} cm^{-3} was successively grown on the top of the heterostructures with Si substrate (see Fig. 1). The TEM was used to observe the thickness of the epitaxial layers and the dislocation distribution.

3. Results and discussions

Figure 2(a) shows the 3.0 μm GaAs layer and 15 pairs AlGaAs/GaAs superlattice (SL) which were grown by MOVPE on $Ge/Si_xGe_{1-x}/Si$ substrate. On the top of the undoped GaAs layer, a MESFET structure with a 1500 Å channel doped at 5×10^{17} cm^{-3} and 500 Å contact layer doped at 5×10^{18} cm^{-3} was grown. The strained AlGaAs/GaAs superlattice layers will improve the surface roughness.[3] Fig. 2(b) shows the cross-section TEM image of the SiGe buffer layers grown on Si substrate. The total thickness of the epitaxial structure is only approximately 2.6 μm. There were a

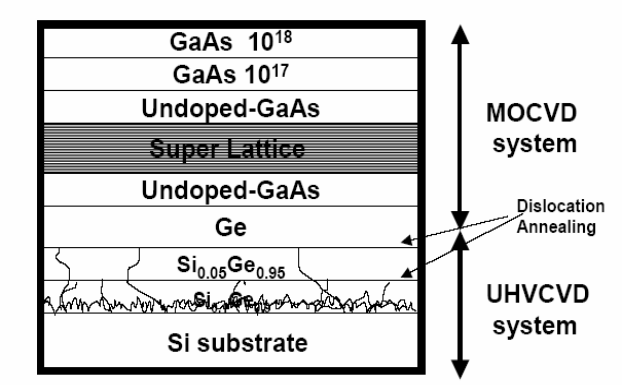
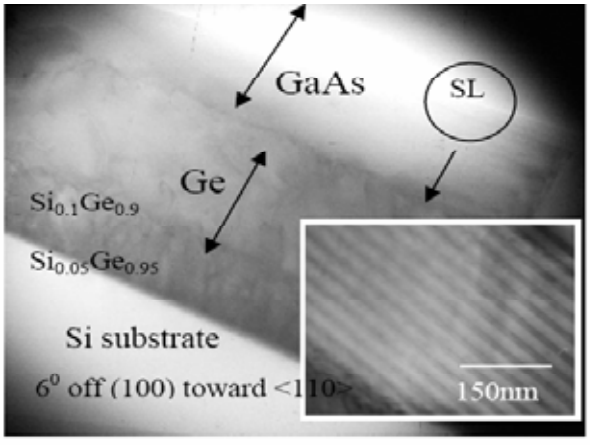
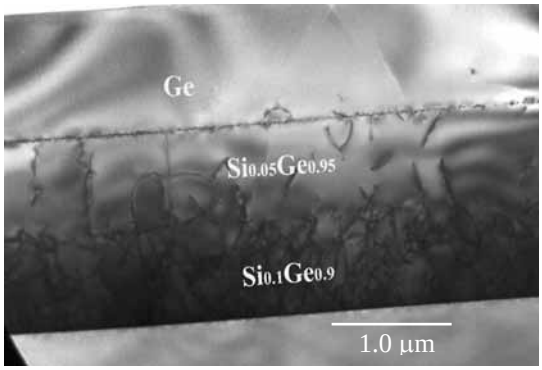


Fig. 1. Schematic diagram of GaAs MESFETs on Si substrate

large number of dislocations located near the $Si_{0.1}Ge_{0.9}$/Si interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer. The upward propagated dislocations were bent sideward and terminated very effectively by the $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$ interfaces. Almost no threading dislocation can propagate into the top Ge layer. Fig. 3a shows the double-crystal x-ray diffraction patterns of the Ge layer and



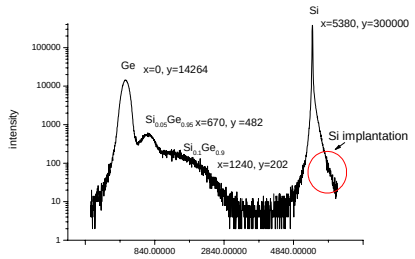
(a)



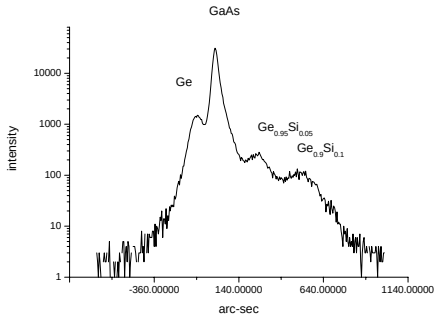
(b)

Fig. 2. Transmission electron micrograph of grown structure with from Si to Ge buffer layer to GaAs transitions. (a) AlGaAs/GaAs superlattice in the GaAs layer. (b) Ge/Si_xGe_{1-x}/Si layer

SiGe layer grown on the Si substrate; the FWHM of Ge peak is 150 arcsec. The wider peaks are attributed to the underlying $Si_{0.05}Ge_{0.95}$ and $Si_{0.1}Ge_{0.9}$ layers. The GaAs layer was grown on Si substrate with 6^0 off (100) toward <110> direction. Its FWHM is 160 arcsec (see in Fig 3b).



(a)



(b)

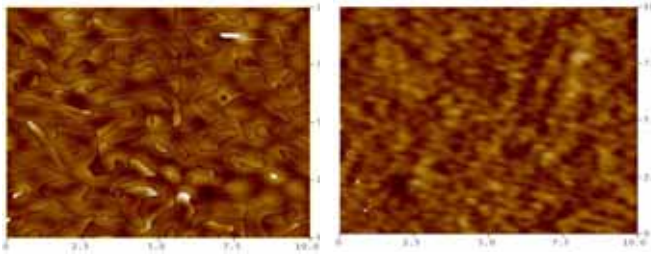
Fig. 3. Double crystal x-ray diffraction pattern of (a)Ge and SiGe layers grown on the Si.substrate (b)GaAs layer grown on Ge/SiGe/Si substrate.

Fig. 4a. reports the GaAs layer grown on the Ge/SiGe/Si substrate with 0^0 offcut. There are two domains differ from each other in a reversal Ga and As atoms in the sublattices resulting in a rotation of 90^0 with respect to the substrate. The two domains were separated by antiphase boundary. Many squared lines were observed on the surface. The root mean square (RMS) was 70.35 Å and the roughness average (Ra) was 60.61 Å. The vertical distances of APBs were 12nm. Fig 4b. is the AFM surface morphology of the GaAs layer grown on the Ge/SiGe/Si substrate with 6^0 offcut. For the substrates with a larger offcut angle, in which the terraces between the steps are very narrow, the steps are so close to each other that no nucleus can be formed on the terraces. As the growth proceeds, the initial nuclei that were grown on the steps will coalesce so that a single domain of GaAs can be achieved [4]. In fig. 4b, no APD was observed on the surface of GaAs layer . The surface roughness was measured by AFM (see Fig. 4b.) The root mean square (RMS) was 7.35 Å and the roughness average (Ra) was 5.81 Å.

The table 1 shows the Hall measured mobility of the GaAs layer grown on the 6^0 offcut Ge/SiGe/Si substrate by using different LT GaAs buffers.

LT GaAs buffer growth temp.	400 °C	430 °C	470 °C
Mobility cm^2/V-s	1024	1690	1520
Concentration cm^{-3}	-4.2E+17	-5.45E+17	-6.3E+17

Table1: The mobility and concentration of the GaAs layergrown with different low- temp GaAs buffers.



(a) (b)

Fig. 4. AFM of the GaAs grown on the composite structure with Ge/Si_xGe_{1-x}/Si sub (a) 0^0 off (b) 6^0 off toward <110>, the scanning area is 10μm×10μm .

4. Conclusions

The Ge/ $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ buffer layer was used to accommodate the strain induced between the Si substrate and the GaAs layer and prevent threading dislocation from propagating into the top GaAs layers. AlGaAs/GaAs supperlattice structure was used to improve the surface roughness and further filter the dislocations in the GaAs layer. The surface roughness RMS of the sample was 7.35 Å and the roughness average was 5.81 Å. The mobility of the GaAs layer grown on the Ge/Si_xGe_{1-x}/Si structure was $1690cm^2$/v-s as the doping concentration was $5.45\times10^{17}/cm^3$. Recently, we even successfully grew an InAs MHEMT structure on this substrate with electron mobility as high as 27300 cm^2/V-s.

References

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