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PL-1 (Plenary)

Nano-CMOS & Emerging Technologies - Myths and Hopes

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1. Introduction

It is now widely recognized that prolongation of CMOS scaling along the roadmap defined by Moore's Law needs additional boosters and new ideas. At the device level, many of those are already recognized [1] and shown to have potential to continue device scaling down to singular nanometers. Though, what we sell to the customer are rather circuits and systems. In contrast with the past, the performance of the latter is less and less governed by the transistor. Therefore, nano-CMOS sets larger challenge for the industry. The improvement of the transistor is still a necessary but no longer the sufficient condition for continuation of the Moore's law.

2. Nano-CMOS

CMOS technology exhibit unprecedented and incommensurable scaling capacity, outperforming with this respect any other known (potential) technology. The smallest MOSFETs are already within the nanometer realm and now hit atomic resolution, Fig. 1. Therefore, competition with CMOS in the field of smallness does not seem to be an easy case.

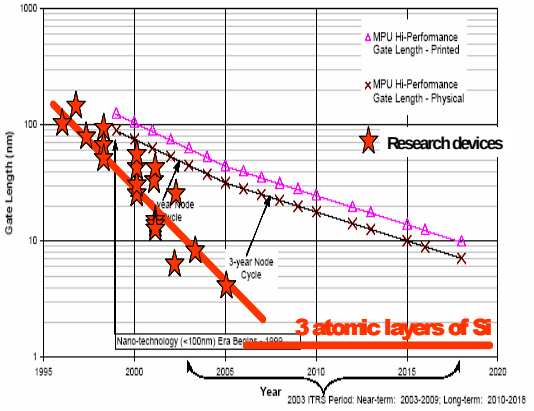


Fig. 1. Experimental CMOS transistors are hitting atomic resolution. Background graph copied from ITRS 2003.

Also regarding the performance of a nano-transistor, CMOS can enjoy satisfaction. Not only have we always been successful in obtaining required by Moore's law performance (during 40 years of scaling), but we also do know how to pursuit on this same path in the future. As shown in Fig. 2, we precisely know how to speed up transistors for the next 15 years by adding new technological boosters. True, the effort is becoming bigger and bigger, Fig. 3, but at least the necessary boosters are known and well defined. Therefore, the risk factor is more economical (cost of their development) than technical (feasibility more or less proven).

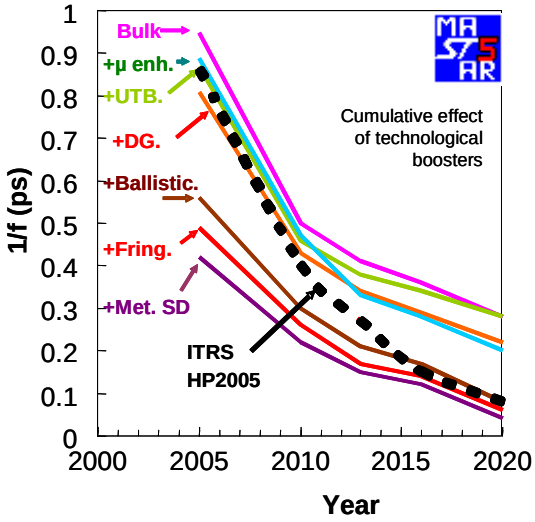


Fig. 2. ITRS Roadmap 2005 as calculated by the PIDS WG (MASTAR program [2]).

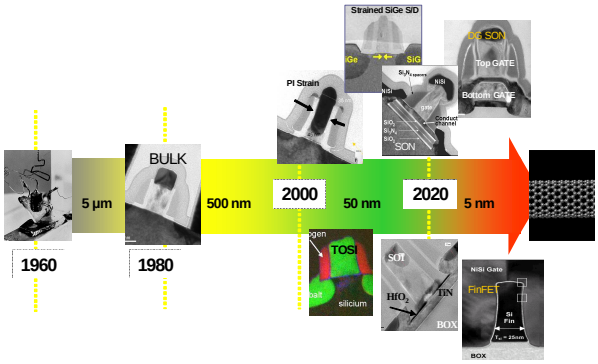


Fig. 3. Burst of non-classical CMOS device structures and materials.

3. Myths

The problem of nano-CMOS does not reside so much in the transistor itself, (on condition we are successful in introducing the appropriate technological boosters in an appropriate time, and can afford doing so). The real problem lies in power dissipation and dispersions. Regarding dispersions, they are due to: (i) - process variations that mainly lead to threshold voltage dispersion and can be

(theoretically and in large portion) suppressed if disposing of devices showing better electrostatic integrity (lower SCE and DIBL); (ii) – random dopant number and distribution. The number of dopants under the gate of nano-transistors is very small, Fig. 4, thus leading to large statistic fluctuations of the threshold voltage.

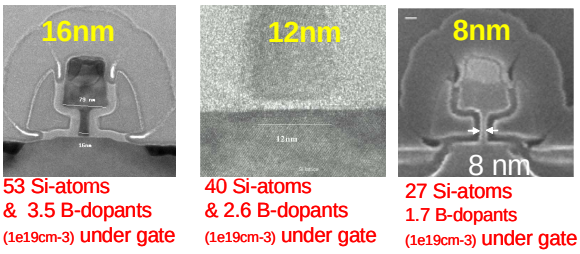


Fig. 4. Continues scaling reveals granularity of the matter.

Taking example of SRAM, the dispersions cause SRAM Static Noise Margin to vanish, Fig. 5, and thus the entire circuit to fail. To prevent this, the designers are obliged to level-off the voltage scaling, Fig. 6, which drastically aggravates the power dissipation problem.

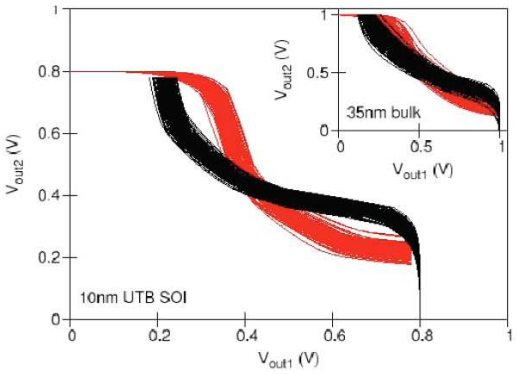


Fig. 5. Vanishing and re-opening SRAM Static Noise Margin due to dispersions within the Bulk and UTB SOI process, respectively – courtesy of Prof. Asen Asenov, Glasgow University, Scotland.

For many types of circuits we are already today at the maximum tolerable power, and due to dispersions, we can hardly reduce Vdd. Therefore, struggling for higher and higher Ion may be a short life-time strategy. The dynamic power is given by:

$$P_{dyn} = nfCV_{dd}^2 = nI_{on}V_{dd}$$

that clearly shows that at constant Vdd any increase in Ion inevitably leads to an increased power dissipation. It is thus very likely that after the euphoric period of development of all kind of stress engineered mobility increase techniques (aiming increased Ion), the priority will be given to devices exhibiting lower dispersions, lower Ioff current, and generally better subthreshold integrity, rather than higher Ion. The tendencies observed in CMOS reinforce the expectation of a prevailing importance of the subthreshold over upthreshold regime. The first tendency is the growing ingredient of portable equipment (vulnerable not only to dynamic but also to static consumption) on the market, and the second that in many circuits the static power is already today approaching the dynamic power level.

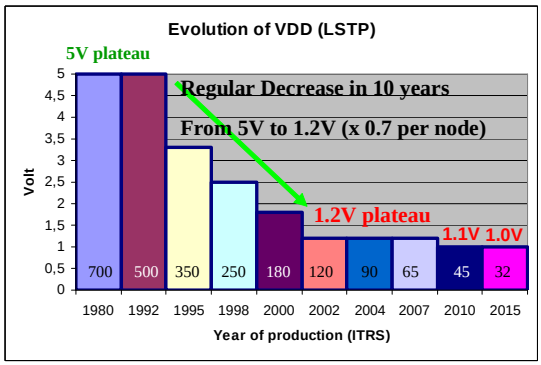


Fig. 6. The Vdd scaling is no longer following the scaling rules thus leading to a drastical aggravation of the power dissipation problem.

Another common belief, that we would rather place among myths, is that high mobility materials bring a radical relief to CMOS scaling. True, higher mobility in III-V materials implies higher Ion current. The gain is, however, counterbalanced by lower DOS (density of states) in these materials, which leads to lower inversion capacitance and thus lower number of inversion carriers [3]. In addition the benefice from higher current faces here the same power problem as described above. The real drawbacks of the III-V materials lie, however, in their inferior electrostatic integrity, that is roughly speaking due to lower DOS, and in their vulnerability to BTBT due to light carrier mass. To give an example, Fig. 7 shows a comparison of subthreshold slopes in III-V based and Silicon based transistors, clearly indicating a superiority of Silicon, with this regard.

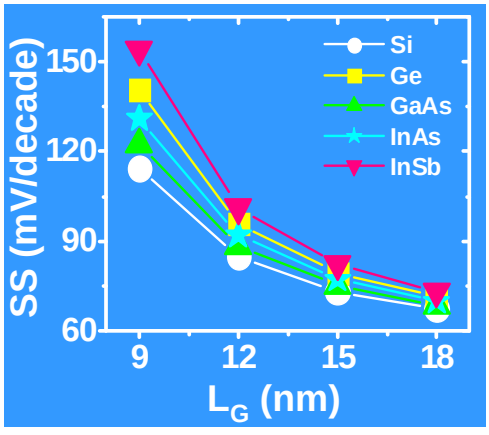


Fig. 7. Simulated subthreshold slope in DG devices with 5nm thick channel for different channel materials – courtesy of Abhijit Pethe, Stanford University.

4. Emerging Technologies

If power is the main issue, what should be expected from emerging technologies is less energy per switch rather than higher speed. The disappointment arises from that nor the former neither the latter shows up in comparison with nano-CMOS, see Fig. 8. Note that the astonishing equality of switching energy, whatever the device structure, may have its source in a similar nature of information treatment. As nicely shown in [4], it is in all cases related to a transfer of charge over a potential barrier that finally leads to the same intrinsic energy expense. As far as the circuit architecture is similar to CMOS, also the extrinsic switching energy will be similar, since irrespective of the switch, a transfer of a bit consists in charging or discharging of the load capacitance. Therefore, if one wishes to escape from this common limitation, a new information treatment, independent of charge transfer is required.

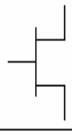
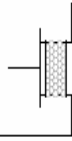
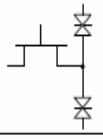
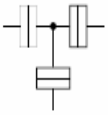
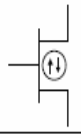
Device		 *FET [B]*	 *1D structures*	 *Resonant Tunneling Devices*	 *SET*	 *Molecular*	 *Ferromagnetic logic*	 *Spin transistor*
Cell Size (spatial pitch)	*Projected*	100 nm	100 nm [C]	100 nm [C]	40 nm [L]	10 nm [Q]	140 nm [U]	100 nm [C]
	Demonstrated	590 nm	~1.5 µm [D]	3µm [H]	~700 nm [M]	~2µm [R]	250 nm [V, W]	100 µm [X]
Density (device/cm^2)	*Projected*	1E10	4.5E9	4.5E9	6E10	1E12	5E9	4.5E9
	Demonstrated	2.8E8	4E7	1E7	2E8	2E7	1.6E9	1E4
Switch Speed	*Projected*	12 THz	6.3 THz [E]	16 THz [I]	10 THz [M]	1 THz [S]	1 GHz [U]	40 GHz [Y]
	Demonstrated	1 THz	200 MHz [F]	700 GHz [J]	2 THz [N]	100 Hz [R]	30 Hz [V, W]	Not known
Circuit Speed	*Projected*	61 GHz	61 GHz [C]	61 GHz [C]	1 GHz [L]	1 GHz [Q]	10 MHz [U]	Not known
	Demonstrated	5.6 GHz	220 Hz [G]	10 GHz [Z]	1 MHz [F]	100 Hz [R]	30 Hz [V]	Not known
Switching Energy, J	*Projected*	3E-18	3E-18	>3E-18	1×10^{-18} [L] [$>1.5\times10^{-17}$] [O]	5E-17 [T]	~1E-17 [V]	3E-18
	Demonstrated	1E-16	1E-11 [G]	1E-13 [K]	8×10^{-17} [P] [$>1.3\times10^{-14}$] [O]	3E-7 [R]	6E-18 [W]	Not known

Fig. 8. Benchmark of Emerging Technologies – from the ITRS 2005 edition.

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5. Hopes

In the past, the 17% improvement-per-year in performance (Moore's law) was driven mainly by a 17% increase-per-year in frequency. This paradigm will have to change now, since it has led circuits to hit maximum tolerable power: 100W, 10W and 1W for HP, LOP and LSTP products, respectively, see Fig. 9. Fortunately, this frequency driven paradigm is not the only possible one. Many design groups at industry and academia work on massive parallelism and other concepts that has potential for providing the same historical improvement in performance (continuation of the Moore's law) without increasing frequency.

Biological systems are the best example of a feasibility of this new paradigm. Human and even animal brain, with their still impressive calculation power [5], are though based on very slow elementary devices (neurons switching frequency is estimated at merely 1kHz).

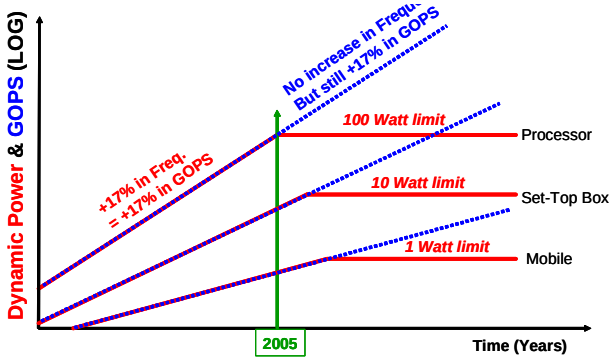

Fig. 9. Power limitation implies the necessity of slowing down (if not stopping) the increase in frequency. GOPS = Giga Operations Per Second.

Conclusions

CMOS is stepping into a new paradigm. Implications at all levels will be significant: (i) - at the device level - less emphasis on Ion current and frequency, whereas much more on the subthreshold regime and matching; (ii) - at the circuit level – multifrequency, multi-supply and other power saving techniques; and (iii) – at the system level – multicore and massively parallel computing . A lot of changes and R&D will be necessary, but the positive message that results from this analysis is that at no level (nor device, neither circuit nor system) CMOS is out of steam. CMOS can thus be expected to remain for long the leading semiconductor technology.

Acknowledgements

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