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Low Threshold Voltage Gate-First pMISFETs with Poly-Si/TiN/HfSiON Stacks Fabricated with PVD-based In-situ Solid Phase Interface Reaction (SPIR) Method

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1. Introduction
Combining metal electrodes with high-k gate dielectrics are a method with some promise for further improving CMOS devices. The gate-first process has great advantages in terms of productivity and device miniaturization, but it requires thermally stable metal/high-k stacks. TiN is a candidate material for p-metal electrodes, and high carrier mobility was reported for pMISFETs fabricated by the replacement gate process. Also, insertion of thin TiN layers between poly-Si electrodes and high-k dielectrics are compatible with the gate-first process [1]. However, WF instability, in which high-temperature annealing results in decreased effective WF toward the Si midgap, is a serious problem. Thus, WF tuning, especially for p-metal electrodes, is required to obtain low Vth metal/high-k devices. In this study, we demonstrate low Vth operation of gate-first pMISFETs with poly-Si/TiN/HfSiON stacks fabricated with a new PVD-based in-situ reaction method and describe how this process improves device performance.

2. Experimental
High-quality, low impurity metal/high-k stacks were prepared with a novel in-situ method that uses a newly developed cluster tool consisting of low-damage PVD equipment and an annealing chamber [2]. The Hf-based dielectrics were formed by a solid phase interface reaction (SPIR) between SiO2 underlayers and metal-Hf deposited by PVD (Fig. 1) [3]. A 0.5-mm-thick Hf layer grown on a RTO-SiO2 (1.8-mm-thick) underlayer was fully consumed by SPIR annealing to form Hf-silicates. Optimized SPIR conditions were adopted based on our previous study [2]. Thin WF metal layers (TIN: 10 · 20 nm) were continuously grown on the high-k dielectrics with the low-damage PVD process. We evaluated sputtering damage and reliability of our PVD system. Excellent film uniformity (1σ=0.18%) and reliability in the nanometer range were obtained (Fig. 2). Damage evaluation using antenna MOS devices revealed that our system is applicable to front end process (Fig. 3).

3. Results and Discussion
3.1 Basic properties of metal/high-k capacitors
Thermal stability of poly-Si/TiN/HfSiON stacks was first investigated using C-V measurement (Fig. 4). EOT of as-deposited HfSiON dielectric (1.02 nm) was thinner than the physical thickness of the initial SiO2 underlayers (1.8 nm). This means that Hf diffusion to the SiO2 underlayer formed Hf-silicate.

4. Conclusion
We demonstrated the use of a new PVD-based in-situ fabrication method for TiN/HfSiON gate stacks. It was found that HfSiON gate dielectrics formed by in-situ SPIR have electrical properties superior to those of conventional CVD-grown films, and that, by reducing the carbon impurity of the stacks, the in-situ metal/high-k process improves Vth and EOT stability even for the gate-first process (spike-RTA at 1050 °C). We successfully fabricated pMISFETs with novel poly-Si/TiN/HfSiON gate stacks that operate at low Vth and have excellent characteristics (Lr=350 μA/μm @L=200 pA/μm) without utilizing mobility enhancement techniques.

References
In-situ SPIR process and poly-Si/TiN/HfSiON fabrication flow. Poly-Si/TiN/HfSiON gate dielectric systems; (a) film uniformity, (b) reliability of HF ultrathin film.

Basic performance of PVD system; (a) film uniformity, (b) reliability of HF ultrathin film.

Fig. 9 Dependence of C-V curves of gate-first pFETs on RTA conditions.

Fig. 10 Dependence of Id-Vg and Ig-Vg curves of pFETs on RTA conditions.

Fig. 11 Dependence of hole mobility of gate-first metal/high-k pMISFETs on RTA conditions.

Fig. 12 Effects of PVD-based in-situ fabrication method and F implantation on Vth tuning.

Fig. 13 Change in hole mobility of gate-first pFETs depending on fabrication method of HfSiON dielectrics and TiN electrodes.

Table 1 Summary of pMISFET performance (Lg/W=4/10μm).

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<thead>
<tr>
<th>Gate stack</th>
<th>Vth (V)</th>
<th>S (mV/dec)</th>
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<tbody>
<tr>
<td>In-situ PVD process</td>
<td>-0.471</td>
<td>65.5</td>
</tr>
<tr>
<td>F implantation</td>
<td>-0.386</td>
<td>69.3</td>
</tr>
<tr>
<td>CVD-metal/high-k</td>
<td>-0.680</td>
<td>65.0</td>
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