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Low Threshold Voltage Gate-First pMISFETs with Poly-Si/TiN/HfSiON Stacks Fabricated with PVD-based In-situ Solid Phase Interface Reaction (SPIR) Method

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1. Introduction

Combining metal electrodes with high-k gate dielectrics are a method with some promise for further improving CMOS devices. The gate-first process has great advantages in terms of productivity and device miniaturization, but it requires thermally stable metal/high-k stacks. TiN is a candidate material for p-metal electrodes, and high carrier mobility was reported for pMISFETs fabricated by the replacement gate process. Also, insertion of thin TiN layers between poly-Si electrodes and high-k dielectrics are compatible with the gate-first process [1]. However, WF instability, in which high-temperature annealing results in decreased effective WF toward the Si midgap, is a serious problem. Thus, WF tuning, especially for p-metal electrodes, is required to obtain low V_{th} metal/high-k devices. In this study, we demonstrate low V_{th} operation of gate-first pMISFETs with poly-Si/TiN/HfSiON stacks fabricated with a new PVD-based in-situ reaction method and describe how this process improves device performance.

2. Experimental

High-quality, low impurity metal/high-k stacks were prepared with a novel in-situ method that uses a newly developed cluster tool consisting of low-damage PVD equipment and an annealing chamber [2]. The Hf-based dielectrics were formed by a solid phase interface reaction (SPIR) between SiO_2 underlayers and metal-Hf deposited by PVD (**Fig. 1**) [3]. A 0.5-nm-thick Hf layer grown on a RTO-SiO_2 (1.8-nm-thick) underlayer was fully consumed by SPIR annealing to form Hf-silicates. Optimized SPIR conditions were adopted based on our pervious study [2]. Thin WF metal layers (TiN: 10 - 20 nm) were continuously grown on the high-k dielectrics with the low-damage PVD without exposure to air, and P-doped poly-Si films (120 nm) were then grown on the WF metal by an ex-situ CVD. MISFETs were fabricated by a conventional gate-first process that includes gate dry etching and spike-RTA up to 1050°C. As previously demonstrated, the above-mentioned process flow is also utilized to fabricate cost-worthy gate-first CMISFETs (poly-Si/TiN for pFETs and TiN removal (doped poly-Si) for nFETs) [1].

We evaluated sputtering damage and reliability of our PVD system. Excellent film uniformity (1σ=0.18%) and reliability in the nanometer range were obtained (**Fig. 2**). Damage evaluation using antenna MOS devices revealed that our system is applicable to front end process (**Fig. 3**).

3. Results and Discussion

3.1 Basic properties of metal/high-k capacitors

Thermal stability of poly-Si/TiN/HfSiON stacks was first investigated using C-V measurement (**Fig. 4**). EOT of as-fabricated HfSiON dielectric (1.02 nm) was thinner than the physical thickness of the initial SiO_2 underlayers (1.8 nm). This means that Hf diffusion to the SiO_2 underlayer formed Hf-silicate. Effective WF of the electrode was 4.80 eV. Note that, after conventional RTA at 1050°C, although the EOT value increased slightly, the TiN was found to retain high effective WF. Also, there was no degradation in gate leakage after annealing (data not shown).

Cross-sectional TEM observation (**Fig. 5**) and high-resolution RBS analysis (**Fig. 6**) revealed that the in-situ SPIR method formed an Hf-rich silicate layer at the upper part of the SiO_2 underlayer and that an initial SiO_2/Si interface was preserved. **Fig. 7** shows XPS spectra taken from the Hf-silicate surfaces. We confirmed nitridation of the silicate surface by reactive sputtering during TiN deposition. These results indicate both formation of HfSiON dielectrics with compositional gradation and preservation of high-quality SiO_2/Si bottom interface. **Fig. 8** represents SIMS depth profiles of the gate stacks. The results from the in-situ and ex-situ processes (air exposure for 24 hours before TiN deposition) make it obvious that the PVD-based in-situ process minimized carbon impurities both within the HfSiON layer and metal/high-k interface. Since carbon impurities form electrical defects in Hf-based oxides [4], we can expect improved electrical properties from the in-situ process.

3.2 Performance of gate-first pMISFETs

The effects of RTA temperature on performances of pMISFETs with poly-Si/TiN/HfSiON gate stacks are shown in **Figs. 9 - 11**. Because of the improved thermal stability induced by the in-situ SPIR method and poly-Si capping layers, EOT increase was suppressed even after the gate-first process (EOT=1.36 nm @1050°C), and V_{th} was stable at this temperature range (**Fig. 9**). **Fig. 10** represents V_g versus I_d and I_g curves, which showing normal transistor operation and reasonably small gate leakage. Hole mobility was improved by high-temperature RTA (**Fig. 11**). These results demonstrate the advantages of our novel poly-Si/TiN/HfSiON stacks in terms of V_{th} stability, EOT scaling, and carrier mobility, which also satisfy requirements as a gate-first CMIS process.

Fluorine (F) implantation into substrates is effective in controlling V_{th} of high-k pFETs [1]. However, excess F degrades transistor performance. Thus, it should be combined with another V_{th} tuning technique. **Fig. 12** shows our scenario for achieving low V_{th} pMISFETs. As previously reported, we observed V_{th} shift toward the Si midgap and an EOT increase for the CVD-based ex-situ process (CVD-TiN/CVD-HfSiON). Our results clearly indicate that combining light F implantation with the novel in-situ SPIR process is a realistic method of V_{th} tuning. **Fig. 13** also shows change in hole mobility depending on gate stack fabrication method. HfSiON gate dielectrics prepared with the in-situ SPIR method show hole mobility superior to that of conventional CVD-grown gate stacks, and continuous TiN deposition without air exposure improves carrier mobility. As listed in **Table 1**, we obtained an excellent subthreshold swing for pFETs fabricated with the in-situ method and demonstrated the use of light F implantation to obtain low V_{th} without severe degradation of subthreshold characteristics.

Fig. 14 shows the V_{th} roll-off characteristics of pMISFET with poly-Si/TiN/HfSiON gate stacks. The V_{th} of long channel devices is successfully suppressed at about 0.43 V without F implantation, and short channel devises are also well behaved. **Fig. 15** shows I_{on}-I_{off} characteristics of pFETs. We obtained excellent current drivability for the metal/high-k gate stacks (I_{on}=350 μA/μm @I_{off}=200 pA/μm) without utilizing mobility enhancement techniques.

4. Conclusion

We demonstrated the use of a new PVD-based in-situ fabrication method for TiN/HfSiON gate stacks. It was found that HfSiON gate dielectrics formed by in-situ SPIR have electrical properties superior to those of conventional CVD-grown films, and that, by reducing the carbon impurity of the stacks, the in-situ metal/high-k process improves V_{th} and EOT stability even for the gate-first process (spike-RTA at 1050°C). We successfully fabricated pMISFETs with novel poly-Si/TiN/HfSiON gate stacks that operate at low V_{th} and have excellent I_{on}-I_{off} characteristics (I_{on}=350 μA/μm @ I_{off}=200 pA/μm).

References

[1] for example T. Hayashi *et al., IEDM Tech. Dig.*, p.247, 2006. [2] S. Horie *et al., Ext. Abstr. SSDM,* p.414, 2006. [3] H. Watanabe *et al., Appl. Phys. Lett.* **85**, 451 (2004). [4] T. Kawahara *et al., Jpn. J. Appl. Phys.* **43**, 4129 (2004).

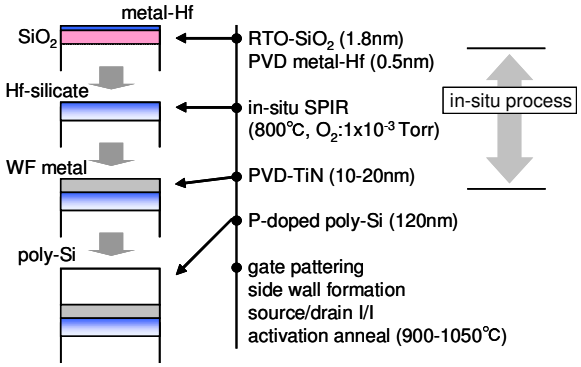

Fig. 1 Concept and fabrication flow of poly-Si/TiN/HfSiON gate stacks with PVD-based in-situ SPIR method.

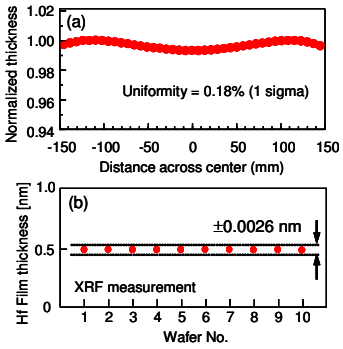

Fig. 2 Basic performance of PVD system; (a) film uniformity, (b) reliability of Hf ultrathin film.

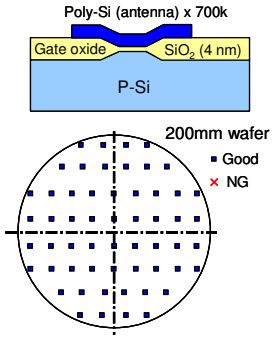

Fig. 3 Damage characterization using antenna MOS capacitors. Antenna ratio was 700k.

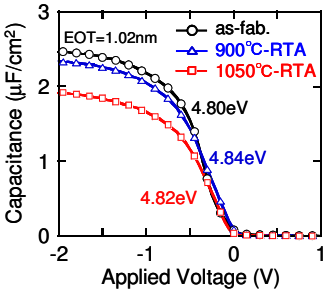

Fig. 4 C-V curves of metal/high-k capacitors fabricated with PVD-based in-situ fabrication method before and after RTA (900, 1050℃).

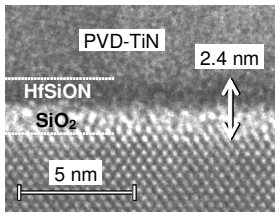

Fig. 5 Cross-sectional TEM image of TiN/HfSiON/SiO_2/Si stacks.

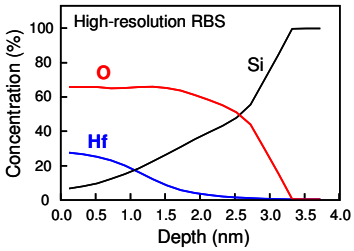

Fig. 6 Depth profile of HfSiON gate dielectric fabricated with in-situ SPIR.

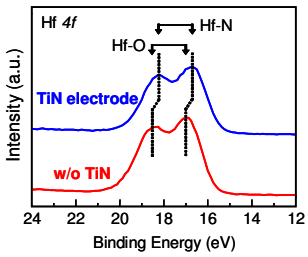

Fig. 7 XPS analysis of Hf-silicates; (a) as-fabricated Hf-silicate surface, (b) after TiN growth (TiN overlayer was removed by wet etching).

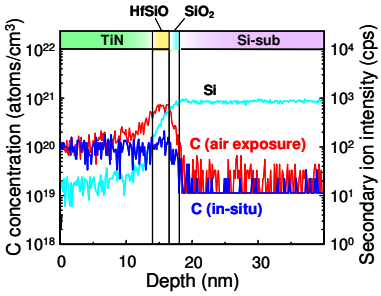

Fig. 8 SIMS profiles of carbon impurity of TiN/HfSiON/SiO_2 stacks.

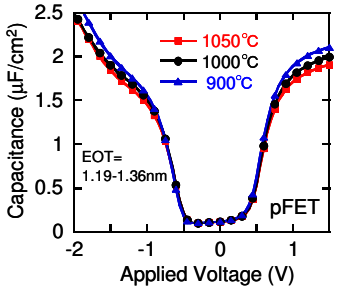

Fig. 9 Dependence of C-V curves of gate-first pFETs on RTA conditions.

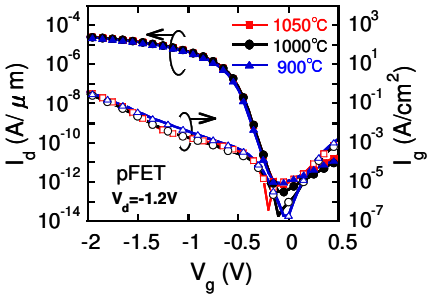

Fig. 10 Dependence of Id-Vg and Ig-Vg curves of pFETs on RTA conditions.

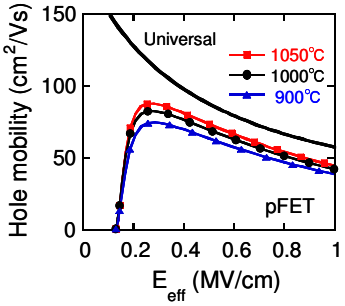

Fig. 11 Dependence of hole mobility of gate-first metal/high-k pMISFETs on RTA conditions.

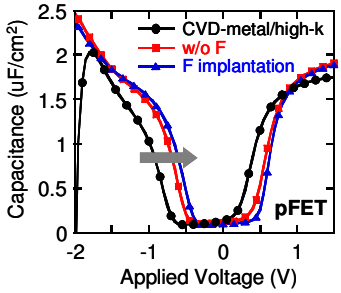

Fig. 12 Effects of PVD-based in-situ fabrication method and F implantation on Vth tuning.

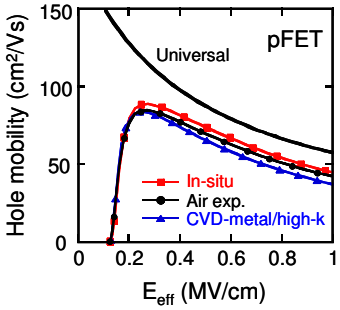

Fig. 13 Change in hole mobility of gate-first pFETs depending on fabrication method of HfSiON dielectrics and TiN electrodes.

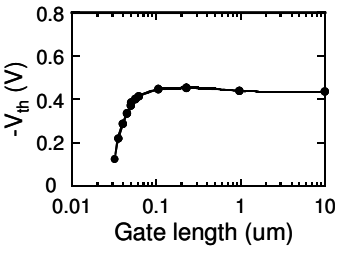

Fig. 14 Vth roll-off characterisitics of pMISFET with poly-Si/TiN/HfSiON gate stacks.

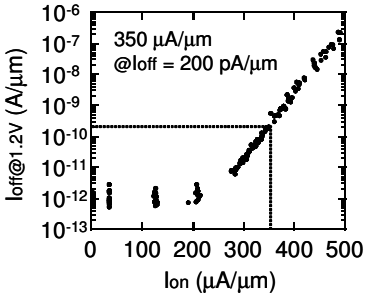

Fig. 15 Ion-Ioff characteristics of pMISFET with poly-Si/TiN/HfSiON gate stacks.

Table 1 Summary of pMISFET performance (Lg/W=4/10μm).

Gate stack	Vth (V)	S (mV/dec)
In-situ PVD process	-0.471	65.5
F implantation	-0.386	69.3
CVD-metal/high-k	-0.680	65.0