A-1-5 Gate First PFET Poly-Si/TiN/Al₂O₃ Gate Stacks with Inversion Thicknesses Less than 15Å for High Performance or Low Power CMOS Applications

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Abstract

Aluminum Oxide (Al₂O₃) is evaluated as a gate dielectric in conjunction with TiN metal in a PFET gate first process flow. We have fabricated high performance PFET stacks with effective work functions 220 mV from band edge without counter doping or additional implants. The most aggressive stacks scale below inversion thicknesses (T_{inv}) of 15Å with less than 10% mobility loss. At T_{inv} = 14.3Å the gate leakage (J_g) is 9.8 A/cm². Optimized stacks achieve the highest reported PFET drive currents without stress elements (867 μ A/ μ m at an off current of 30 nA/ μ m, V_{dd} = 1.3V). Alternatively, thickening the Al₂O₃ layer creates a stack suitable for low power applications with a T_{inv} = 19Å and a J_g = 0.05 A/cm². *Introduction*

Continued scaling of planar CMOS technology requires metal gate and high-k to further scale inversion thicknesses (T_{inv}) beyond the poly-Si/SiON limit of ~20Å. Initially, many groups attempted Al₂O₃ with poly-Si gates, but boron penetration in PFETs, poor mobility and threshold voltage (V₁) control prevented success [1].

Since then, Hafnium (Hf) based dielectrics have emerged as leading high-k dielectric candidates. Band edge nFET solutions, with near ideal mobility, have been fabricated with Hf-based dielectrics [2], but fabricating a thin T_{inv} gate first stack with a work function appropriate for PFETs has been elusive. Hafnium Oxide (HfO₂) pins the effective work function of the gate stack about 700 mV from PFET band edge, possibly due to oxygen vacancies in the dielectric. The effective work function may be shifted up to 300 mV towards PFET band edge by depositing an Al₂O₃ cap layer on top of the HfO₂ gate dielectric [3,4]. The best reported stack with Al₂O₃ caps is still ~400 mV from PFET band edge with a $T_{inv} = 16\text{\AA}$ [3]. In addition to increasing the T_{inv}, the Al₂O₃ cap layer dramatically reduces hole mobility and unacceptably increases the Negative Bias Temperature Instability (NBTI) [3, 4]. Since it is known that aluminum and Hf interdiffuse [5], it is surmised that this interaction causes the detrimental electrical characteristics. Alternatively, a replacement gate process has achieved near band edge effective work functions at $T_{inv} = 17$ Å [6], but the replacement gate process poses a formidable integration challenge for aggressively scaled channel lengths.

In this paper, we present the electrical characteristics of gate stacks consisting of an SiO₂ interfacial layer, Al_2O_3 dielectric layer, and a TiN metal gate in a gate first process. Thus, we completely eliminate HfO₂ from the PFET gate stack. By optimizing the thickness of interfacial layer and the Al_2O_3 , we achieve mobility and reliability comparable to non-capped Hf-based stacks with the added benefit of an effective work function 220 mV from PFET band edge. *Experimental Details*

Fig. 1 depicts the process flow. The gate stack consists of an SiO_2 interface/Al₂O₃/TiN/poly-Si. Four different SiO₂ interface thicknesses (IL) were grown, with IL 4 being the thickest and IL 1 being the thinnest. The Al₂O₃ was deposited by ALD or PVD with thicknesses varying from 5Å to 24Å. The PFETs were fabricated in a gate first self-aligned flow with a 985°C, 5 s source/drain RTA. HfO₂/TiN/poly-Si and 20Å SiO₂/poly-Si stacks were fabricated for comparison [7]. The PFETs were fabricated on (100) silicon without embedded silicon germanium source/drain, counter doping, or any non-traditional implants.

Long Channel Results

The C-V and I_d -V_g for two aggressively scaled stacks are shown in Figs. 2 and 3. The T_{inv} are ~14.3Å and 15Å, while both V_t are 220 mV from the poly-Si/SiO₂ control. There is negligible fixed charge in the Al₂O₃ stacks, illustrated by the independence of V_t with Al₂O₃ thickness (Fig. 4). The effective work function, ~4.98 eV, is near the theoretical work function of TiN [8]. This contrasts with the HfO₂ stack, which generates a V_t of -700 mV. The lack of distributed bulk fixed charge in Al₂O₃ may be attributable to the covalent bonding in Al₂O₃. This contrasts with the ionic nature of HfO2 which may be the cause of the large oxygen vacancy concentration that plagues HfO₂. The Al₂O₃ dielectrics are superior to Al₂O₃ capped HfO₂ dielectrics, which, at best, have effective work functions ~4.8eV for thin T_{inv} . Figs. 6 and 7 compare peak and high field mobility as a function of IL and Al₂O₃ thickness. The thinnest IL exhibit a mobility reduction, while the thicker IL have comparable (or higher) mobilities to the HfO₂ control stack. The Al₂O₃ dielectric must be separated from the channel by some minimum distance to achieve high mobilities. The mobility loss is not due to interface states, since charge pumping measurements verify low trap densities $(\sim 6x10^{10}/cm^2)$ for all stacks (Fig. 8). An IL dependent mobility was reported for poly-Si gated Al₂O₃ and attributed to remote Coulomb scattering [9]. This data suggests that remote Coulomb scattering also limits mobility in Al₂O₃ metal gated structures.

Because of the moderate dielectric constant, J_g is an obvious concern for aggressively scaled Al_2O_3 dielectrics. Nevertheless, four orders of magnitude leakage reduction is maintained down to $T_{inv} = 14.3$ Å with $J_g = 9.8$ A/cm² (Fig. 9), which is suitable for high performance technologies. For low power technologies, J_g reduces to 0.05 A/cm² at a T_{inv} of 19Å.

Performance

Fig. 10 compares long channel linear drive current (I_{dlin}) at constant overdrive ($V_t + 800 \text{ mV}$) for Al_2O_3 and HfO_2 stacks. The thinner Al_2O_3 stacks are within 5% of the linear drive performance of the HfO_2 . Short channel devices down to 70 nm were fabricated with an optimized stack. The process did not include counter doping, fluorine implants, or any other artificial means of affecting the effective work function. Roll-off and DIBL are shown in Fig. 11. DIBL is well controlled down to 70 nm, with a DIBL of 68 mV/V. The highest reported on-currents for (100) PFETs without stress elements have been achieved with an on-current (I_{on}) of 742/867 μ A/ μ m at an off current (I_{off}) of 20/30 nA/ μ m for a 1.2/1.3V power supply, respectively (Fig. 12). Table I compares the drive currents achieved in this work with recent published literature. **Reliability**

The poly-Si/TiN/HfO₂ stack suffers from comparable NBTI degradation as a poly-Si/SiON stack ($T_{inv} = 20$ Å) [10], while NBTI is quite poor for the Al₂O₃ capped HfO₂ dielectrics [3]. Fig. 13 shows that the poly-Si/TiN/Al₂O₃ stack ($T_{inv} = 15$ Å) has comparable NBTI as the control samples and therefore should meet NBTI reliability. *Conclusions*

Poly-Si/TiN/Al₂O₃ gate stack has been demonstrated to be a strong PFET candidate in a gate first integration for both high performance and low power applications. By optimizing the Al₂O₃ and interface thicknesses, T_{inv} has been scaled below 15Å with mobility and reliability equal to HfO₂ based stacks, while the effective work function has been improved to ~220 mV from PFET band edge. Aggressive T_{inv} scaling combined with record I_{on} demonstrate the viability of Al₂O₃ as a gate dielectric for future CMOS applications.

References: [1] D. A. Buchanan, *et al. IEDM*, pg. 223 (2000). [2] V. Narayanan *et al.*, *VLSI*, pg. 178 (2006). [3] S.C. Song *et al.*, *VLSI*, pg. 13 (2006). [4] H. Jung, *et al.*, *VLSI*, pg. 232 (2005). [5] L. Miotti, *et al.*, *APL*, in press. [6] S. Yamaguchi, *et al.*, *VLSI*, pg. 152 (2006). [7] V. Narayanan *et al.*, *EDL*, Vol. 27, No. 7, pg. 591 (2005). [8] V. K. Paruchuri, unpublished. [9] S. Saito, *et al.*, JAP 98, 113706 (2005). [10] S. Zafar, *et al.*, *VLSI*, pg. 23 (2006). [11] B. Doris *et al.*, *VLSI*, p. 214 (2005). [12] R. Chau et al., *EDL*, Vol. 25, No. 6, pg 408 (2004). [13] W. J. Taylor Jr., et al., IEDM, pg. 625 (2006).



Fig. 1 Process flow and schematic of the PFET gate stack.



Fig. 2 Inversion Split C-V comparing SiO_2 with HfO_2 and Al_2O_3 dielectrics. The Al_2O_3 /TiN stack is only 220 mV shifted from the poly-Si/SiO₂ reference.



Fig. 4 V_t as a function of Al_2O_3 thickness. The independence of V_t with respect to dielectric thickness implies low bulk fixed charge in the Al_2O_3 dielectric.



Fig. 5 V_t as function of T_{inv} . TiN/Al₂O₃ stacks scale down to 15Å without change in effective work function.



Fig. 6 The mobility of optimized TiN/ Al_2O_3 stacks equal the TiN/HfO₂ control stack and are within 10% of the universal mobility.



Fig. 7 TiN/Al_2O_3 stacks suffer mobility degradation for the thinnest interfaces, but exhibit minimal degradation for the slightly thicker interfaces.



Fig. 8 Charge pumping reveals that interface trap density is independent of interface thickness.



Fig. 9 Al₂O₃ stacks targeted towards high performance still exhibit greater than 4 orders of magnitude leakage reduction down to $T_{inv} = 14.3$ Å.

Table I. Comparison to published high-k/Metal Gate PFET data.

	This Work	This Work	ref. [11]	ref. [12]	ref. [13]	ref. [6]	ref. [6]	ref. [4]
Vdd (V)	1.2	1.3	1.3	1.3	1.2	1.2	1	1.2
lon(μA/mm)	489/587/742	694/867	770	710	570	583	265	250
loff(nA/mm)	0.02/1.5/20	2.5/30	28	45	1	1	1	0.02
Lgate (nm)	70	70	50	80	40	60	60	unknown
Gate First	yes	yes	yes	unknown	yes	no	no	yes
Substrate	bulk	bulk	FDSOI	bulk	SOI	bulk (110)	bulk	unknown
Gate Stack	Al2O3/TiN	Al2O3/TiN	HfO2/unknown	HfO2/unknown	HfO2/TaC	HfO2/Ru	HfO2/Ru	HfSiO/Al203/TaN



Fig. 10 The reciprocal of T_{inv} vs. linear drive current. The best Al_2O_3 stacks are within 5% of the TiN/HfO₂ reference stack.



Fig. 11 Roll-off and DIBL are well controlled down to 70 nm gate lengths for the optimized stack.



Fig. 12 I_{on}/I_{off} for 1.2 and 1.3 bias voltages. The optimized stack drives 867 μ A/ μ m at an I_{off} of 30 nA/ μ m at 1.3V supply voltage.



Fig. 13 TiN/Al_2O_3 exhibits similar NBTI behavior as the control stacks [10].