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Evaluation of $SiO_2/GeO_2/Ge$ MIS Interface Properties by Low Temperature Conductance Method

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1. Introduction

Ge-channel MOSFETs have been proposed as one of the candidates of device structures over the scaling limit of Si technology because of the high carrier mobility than Si (2x for electrons and 4x for holes). On the other hand, the realization of the superior MIS interfaces is one of the most critical issues on Ge MOSFETs. However, their interface properties have not been investigated in detail. Particularly, it has recently been reported that interface states densities of Ge (D_{it}) near the conduction band are high [1], which can be an essential reason for low mobility in Ge n-channel MOSFETs and, thus, a fatal problem for Ge CMOS. They have evaluated D_{it} near the band edge by using low temperature conductance method. It is still necessary, however, to examine the accuracy and the validity of the results, because they used only n-type Ge substrate MIS capacitors for measuring the interface states near both conduction and valence bands and the measurement temperature only at 80 K. In this study, thus, we systematically evaluate the energy distribution of D_{it} and the dynamic properties of the interface states up to near the band edge by applying the low temperature conductance method to n- and p-type Ge MIS capacitors in a wide range of measurement temperatures.

In this paper, $SiO_2/GeO_2/Ge$ MIS interfaces are evaluated. This is because SiO_2/SiGe MIS structures formed by the Ge-condensation method have been reported to have superior interfaces so as to provide the hole mobility of 10 times as high as the universal one [2] and also we have already presented the good interface characteristics by forming GeO_2 between SiO_2 and Ge substrates [3].

2. Samples Fabrication

The fabrication flow is shown in Fig. 1 [3]. SiO_2/GeO_2/Ge MIS capacitors were fabricated on (100) oriented n- and p-type Ge substrates. Cyclic HF (buffered HF) dip with DI water was used to remove Ge native oxides. Si films of as thin as 1.2-1.5 nm were grown at 100 °C by MBE. Subsequently, the samples were oxidized at 200 °C in O_2 plasma for 120min. The oxidation time, when Si was fully oxidized and GeO_2 between SiO_2 and Ge substrate was formed, was determined by XPS analyses. Finally, Al films were deposited to form gate electrodes.

3. Results and Discussions

In order to evaluate the energy distributions of D_{it}, the surface potential corresponding to each conductance peak needs to be accurately determined. For this purpose, one-to one relationship between the capacitance under high frequency limit and the surface potential is utilized. Fig.2 shows the frequency dependence of the capacitance at various temperatures. It is found that the frequency dispersion over 100 kHz is hardly observed at less than 221 K, meaning that we can regard the C-V curves at less than 221 K as the high-frequency C-V curves.

Here, the upper or lower limit of the surface potential where D_{it} can be measured, in other words, the minimum value between the surface potential and the band edges is determined by the potential, where the conductance peak locates at the upper limit of the measurement frequency, 1 MHz in this study. Fig. 3 shows this minimum value of the surface potential as a function of the measurement temperature. It is confirmed that, as the temperature decreases, the D_{it} measurement is possible up to the surface potentials closer to the band edges. The energy distributions of interface states densities for SiO_2/GeO_2/n-type Ge and p-type Ge MIS capacitors are shown in Fig. 4 (a) and (b), respectively. Here, the effects of the surface potential fluctuation on the conductance are taken into account in evaluating D_{it}. It is found that D_{it} increases monotonically as the surface potential moves from the valence band edge to the conduction band edge. The minimum value of D_{it} is estimated to be in the order of $10^{11}eV^{-1}cm^{-2}$ near the valence band edge. Also, the higher D_{it} near the conduction band edge, claimed in [1], is also observed for the present Ge MIS capacitors.

Fig.5 shows the temperature dependence of the time constant of the interface states evaluated from the frequency at the conductance peak. It is found the slope of the time constant in the logarithm plot increases with a decrease in the temperature. As for Si MOS interfaces, the time constant is known to be described by

$$\tau = (1/\sigma v_{th} N_B)\exp(q\phi/k_B T) \qquad (1)$$

As seen in Fig.6, however, the slope of the time constants of both p- and n-type samples is not represented by $q/k_B T$, predicted on a basis of (1). This fact suggests the energy and/or temperature dependence of the capture cross sections or the relevance of any other processes than the simple capture/emission process of the majority carriers.

In order to modify D_{it}, annealing after metal gate formation (PMA) using N_2, H_2 and atomic hydrogen are carried out. The annealing temperature and time are 300°C and 30 min, respectively. The energy distribution of D_{it} is shown in Fig.7. It is found that the H_2 and atomic hydrogen annealing cause the increase in D_{it}, while the N_2 annealing lead to almost no change in D_{it}. This fact indicates that hydrogen deteriorates the Ge MIS interfaces at least under the present condition.

4. Conclusion

The systematic evaluation of Ge MIS interface properties was carried out by using the $SiO_2/GeO_2/Ge$ MIS structures. The low temperature conductance method was found to be effective in measuring D_{it} near the band edges. The higher D_{it} near the conduction band edge was observed, which could be an essential problem for realizing Ge n-MOSFETs. Also, hydrogen annealing does not work for the present MIS interfaces, though the further optimizations of the annealing process are still needed.

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References [1] K. Martens et al., EDL (2006) 405 [2] T. Tezuka et al., EDL (2005) 243 [3] H.Kumagai et al., SSDM (2006) 398

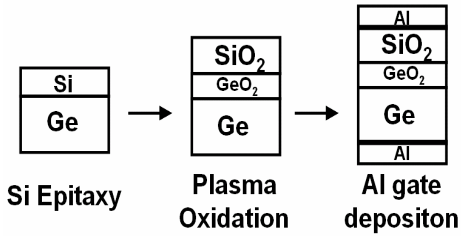

Fig.1 Process flow to fabricate SiO2/GeO2/Ge MIS capacitors by plasma oxidation of ultrathin Si films on Ge.

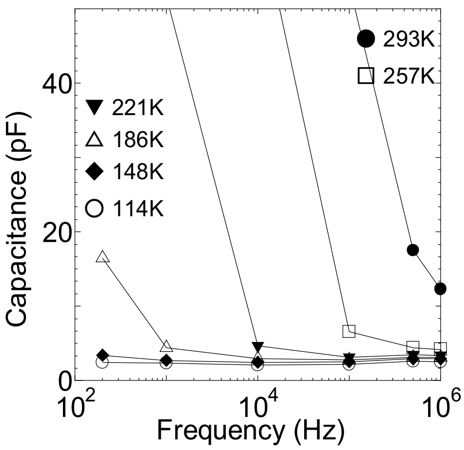

Fig.2 Dependence of capacitances on frequency for the n-type sample at various temperatures.

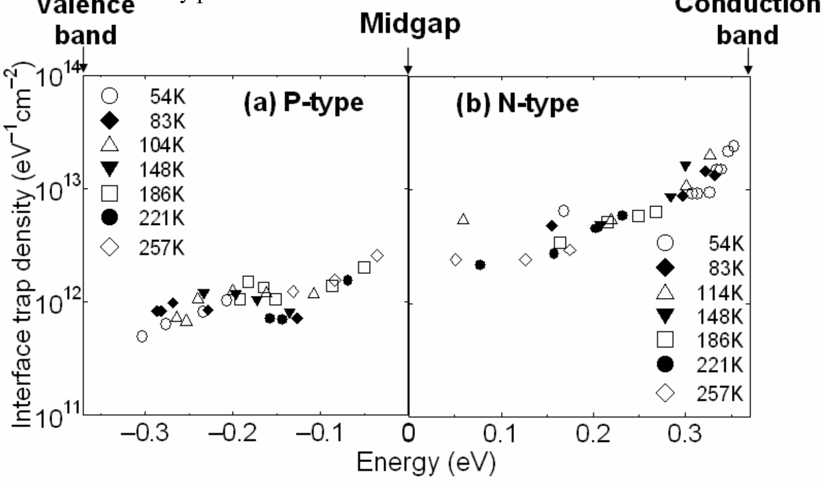

Fig.4 Energy distribution of interface state densities of (a) P-type (b)N-type samples measured at 54K to 257K determined by the conductance method.

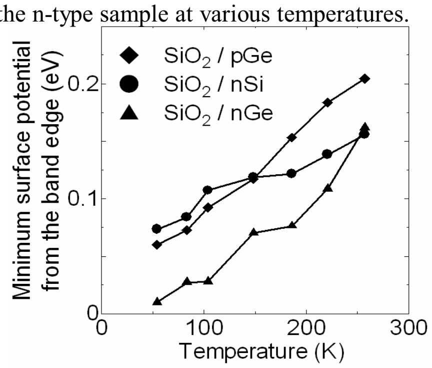

Fig.3 Temperature dependence of minimum surface potential of interface state densities from the band edge.

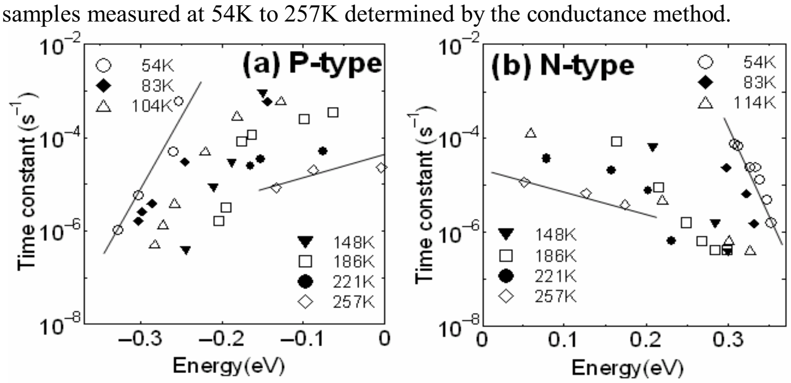

Fig.5 Energy distribution of the time constant determined by frequencies of the conductance peak measured at 54K to 257K.

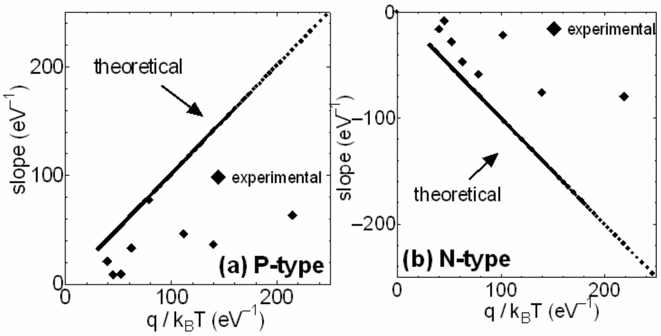

Fig.6 Comparison of slopes of the time constant between the theoretical data with the experimental result.

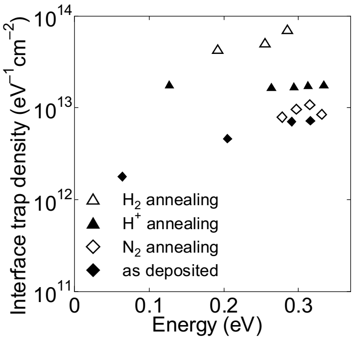

Fig.7 Comparison of interface state densities of samples after annealing by N_2, H_2 and atomic hydrogen measured at 104K.