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Thermally Robust Germanium MIS Gate Stacks with $LaYO_3$ Dielectric Film

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1. Introduction

Germanium has been extensively studied for a material candidate beyond silicon due to its higher carrier mobility [1]. Considering the realization of Ge devices, however, there are several challenging issues to overcome.

(1) High-k materials should be employed for the gate dielectric film to achieve sub-nm EOT for Ge generation.

(2) The process temperature should be above 500 °C in order for the dopants to be fully activated [2].

(3) Inevitably existing Ge-O boding at the Ge/dielectric film interface should be appropriately controlled, which becomes unstable at the Ge interface above 400 ˚C [3]. This instability might degrade its interface properties in high temperature process.

Our group has reported that the interface layer on Ge disappears through the post deposition annealing (PDA) [4]. It may be of a great advantage in terms of EOT scaling. It is concerned, however, that the Ge-O bonding beneath the high-k dielectric film might degrade the interface characteristics due to the easy desorption of GeO through the PDA. Furthermore, they have recently found that Y_2O_3 (k~11) shows relatively favorable characteristics on Ge even in the case of 600 °C PDA [5], but its k-value is not enough for a required EOT in Ge device generation. Therefore, this work intends to find a new way to solve those challenges by introducing new materials and processes. This paper proposes $LaYO_3$ (LYO) with k_{eff}~20 for the gate dielectric film on Ge and the annealing process at 600 ˚C after gate electrode deposition, and demonstrates a dramatic improvement of the interface properties of high-k Ge MIS capacitors.

2. Experimental

LYO films were deposited on HF-last p-type Ge (100) substrates by rf co-sputtering of La_2O_3 and Y_2O_3 in Ar ambient at room temperature. PDA in N_2 ambient was performed at 600°C, followed by Au electrode evaporation to measure the electrical characteristics of MIS capacitors. The crystal structure, composition and thickness of the film were determined with XRD, XPS and GIXR (grazing incident x-ray reflectivity), respectively. Some samples were capped with Si after the film deposition without PDA, followed by Ni evaporation and then silicided at 400~600°C.

3. Results and Discussion

La_2O_3 is a promising high-k material in terms of the k-value and energy band gap for Si-CMOS. **Fig. 1** shows Au/La_2O_3/Ge-MIS C-V characteristics exposed to the air for 0 hour and 24 hours after 600 ˚C PDA. It is found that the C-V characteristic is degraded with the time exposed to the air because La_2O_3 has intrinsically hygroscopic property, which is the same as on Si [6]. However, La_2O_3/Ge interface itself is not so bad if the moisture adsorption is protected. The fact that both Y_2O_3 and La_2O_3 show a better performance suggests that $LaYO_3$ will also provide a good interface with Ge. More favorably, our group has also reported that Y-introduction into La_2O_3 not only improves the hygroscopic behavior but also enhances the permittivity [7]. So, we confirmed the k-enhancement of LYO film on Ge, as shown in **Fig. 2**. This fact means that LYO is a potentially promising material for the higher-k dielectric film on Ge.

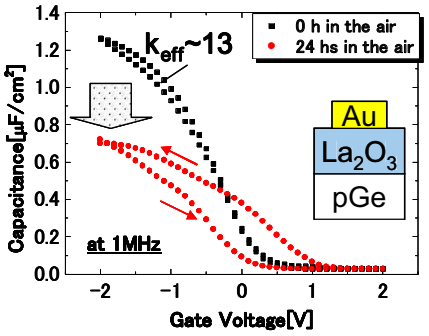

Fig. 1 Comparison of C-V characteristics between La_2O_3/Ge exposed to the air for 0 hour and 24 hours after PDA at 600°C. It is found that the C-V characteristics have been degraded with the time in terms of hysteresis and accumulation capacitance.

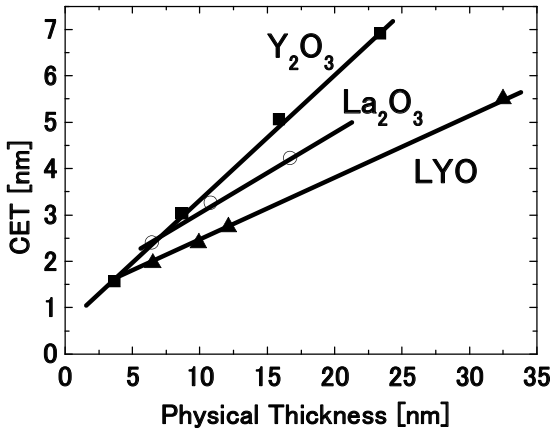

Fig. 2 The relationship between CET and physical film thickness (determined by GIXR) for Y_2O_3, La_2O_3, LYO, annealed at 600°C. The dielectric constant was estimated from the slope. (Y_2O_3: 14.4, La_2O_3: 21.6, LYO: 28.6) It is found that the k-enhancement is achieved using LYO on Ge.

Fig. 3 compares the frequency dependence of normalized capacitance at inversion region (C_{inv}/C_{ox}), which is one of the measures for characterizing the high-k/Ge interface, for Au/high-k/Ge MIS with HfO_2, Y_2O_3, La_2O_3 and LYO annealed at 600 ˚C. It clearly shows that La_2O_3 and LYO are the best among them from the viewpoint of the minority carrier response. However, the C-V characteristics are still

degraded by the interface states even in the case of LYO.

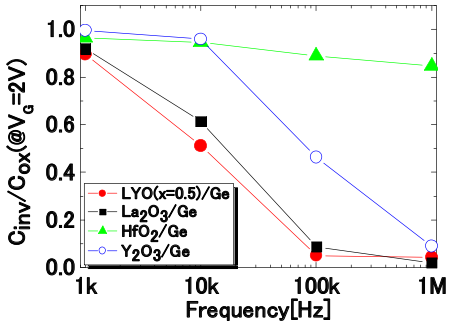

Fig. 3 Frequency dependence of normalized capacitance at inversion region measured for LYO/Ge, La_2O_3/Ge, HfO_2/Ge and Y_2O_3/Ge capacitors annealed at 600°C. While no depletion state is seen in the case of HfO_2/Ge even at 1MHz, LYO and La_2O_3/Ge show relatively much favorable characteristics.

We suspected that this degradation at high-k/ Ge interface might be related to an easy volatilization of GeO, as is the case of ultathin GeO_2/Ge interface [3]. In order to suppress this effect, we propose the FUSI gate technique just after LYO film deposition to stabilize the GeO movement at the interface. The point of this process is that LYO annealing is performed after gate electrode deposition, resulting in a suppression of GeO desorption to the ambient. **Fig. 4** shows C-V characteristics for FUSI/LYO/Ge and Au/PDA-LYO/Ge capacitors annealed at 600 ˚C. In the FUSI/LYO case, a well behaved C-V with a much smaller hysteresis is clearly observed, which means the interface quality is dramatically improved by an appropriate change of the detailed balance of GeO volatilization during FUSI annealing, as schematically shown in **Fig. 5**. Furthermore, the annealing temperature dependence of C-V characteristics for FUSI/LYO/Ge MIS capacitors is shown in **Fig. 6**. It is found that the higher temperature process improves the interface quality as long as below 600˚C. In this process, the high quality GeO_2 layer favorably remains at the interface even after annealing, which contributes to the interface improvement with a very slight penalty of EOT increase. This is striking contrast to the Au/LYO/Ge MIS cases processed by the conventional PDA.

4. Conclusions

Ge MIS capacitors with directly deposited LYO films have been investigated from the viewpoint of the k-enhancement and the Ge interface improvement. Much better C-V characteristics with k_{eff}~20 after 600˚C annealing have been achieved. Moreover, the charge trapping centers have been significantly reduced in FUSI/LYO/Ge MIS capacitors. These dramatic effects will provide a viable process for putting Ge CMOS into practice.

Acknowledgements

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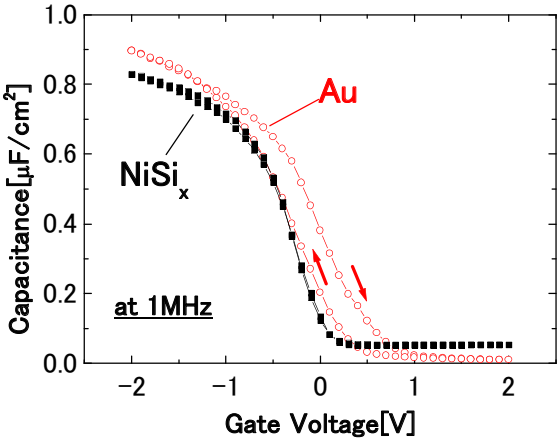

Fig. 4 Bidirectional C-V characteristics measured at 1MHz for the FUSI/LYO/Ge and Au/PDA-LYO/Ge capacitors. It is found that the FUSI gate employment is very effective for reducing hysteresis.

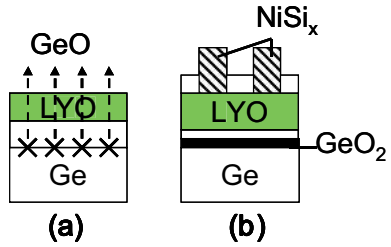

Fig. 5 Schematic picture of the reactions occurring at the interface of **(a)** conventional Au/PDA-LYO and **(b)** FUSI-LYO capacitors. FUSI process is effective for stabilizing Ge interface in (b), while the interface is deteriorated by GeO desorption through the PDA process in (a).

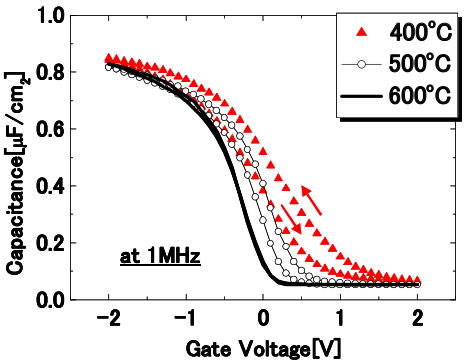

Fig. 6 The effect of silicidation annealing temperature on C-V characteristics. The interface quality is dramatically improved as the temperature increases, in terms of hysteresis, interface states and flat-band voltage.

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