Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 28-29

A-2-6

Effects of Sulfur Passivation on Ge MOS Capacitors with High-k Gate Dielectric

Ruilong Xie and Chunxiang Zhu*
Silicon Nano Device Lab, Dept of Electrical and Computer Engineering
National University of Singapore, 10 Kent Ridge Crescent, Singapore
(*Phone: +65-65168930 *Email: elezhucx@nus.edu.sg)

1. Introduction

Germanium (Ge) substrate is increasingly being studied for MOSFET applications because of its high intrinsic carrier mobilities [1]. The lack of a stable Ge oxide makes it difficult to fabricate a Ge MOSFET. However, the emergence of high-k dielectric gives opportunity to fabricate devices having both merits of high-k and Ge. To have a high quality high-k gate stack on Ge substrate, minimizing the GeO_x at the surface between the high-k and substrate is a critical issue and Ge surface passivation is needed before gate stack formation. Most work so far has concentrated on nitridation using NH_3 gas treatment [2] or atomic N exposure [3], where nitrogen is introduced into the interface of germanium oxide to passivate the germanium. However, they still exhibit high interface state density ($D_{it} > 10^{12}$ cm^{-2}) [2，3]. Recently, Martin M. Frank *et al* [4] reported the Ge MOS capacitors with sulfur (S) passivation by aqueous $(NH_4)_2S$ treatment. It was found that interface state density is lower than NH_3 nitridation passivated samples. However, the gate stack did not go through any high temperature annealing (e.g. >400°C). Also, there is no report on electrical properties like EOT and gate leakage current. In this study, we show that sulfur passivation can reduce the EOT of gate stack while maintain the gate leakage current, moreover, it can improve the thermal stability of the Ge/high-k interface.

2. Experiment

The starting wafers were n-type Ge wafers (Sb doped, R= 0.04-0.08Ωcm). The native oxide was removed by a cyclic rinsing between deionized water and diluted HF [5]. The substrates were then immersed into aqueous $(NH_4)_2S$ solution for 30 mins, followed by a water rinse and a N_2 blow dry. Control samples with only HF cyclic rinsing were also prepared. After that, HfO_xN_y was then formed on both types of samples by HfON deposition with reactive sputtering and post deposition annealing in an N_2 ambient at 500°C for 1 min. A 150nm TaN gate electrode was then sputtered. This was followed by lithography and dry etching processes. Post metal annealing (PMA) at different temperatures was then performed for thermal stability investigation. The final step was forming gas anneal in $H_2 + N_2$ ambient at 420ºC for 2 hours.

3. Results and Discussion

Sulfur incorporation on Ge surface after $(NH_4)_2S$ treatment is conformed by the peak (~162eV) in the S 2p signal in Fig 1. The inset of N 1s spectra shows that N would not be introduced to Ge surface by $(NH_4)_2S$ treatment. The XPS data in the Ge 3d region in Fig 2(a) shows that the small peak (signal from 31.5 to 33eV) shifts slightly to the right for samples with S treatment possibly because of the Ge-S peak (29.5 to 30.5eV) overlaps with GeO_2 peak (~32.5eV). To further investigate the surface chemical states after the pre-gate cleaning/treatment, the Ge 2p spectrum is shown in Fig 2 (b). The shoulder (1219~1221eV), for the samples only cleaned by HF, is attributed to GeO_x ($x \leq 2$) bonds, which are believed to be introduced during the sample transportation [2]. For the sample treated by $(NH_4)_2S$, the size of the shoulder is smaller. Considering the possible bonds that Ge atom may have, curve fitting result shows that the shoulder consists of Ge-O (1220.2eV) and Ge-S (1219.8eV) bonds, so the $(NH_4)_2S$ treatment can reduce Ge-O bonds on the surface.

Fig 3 shows the *C-V* characteristics of the MOS capacitors (a)with $(NH_4)_2S$ and (b)without $(NH_4)_2S$ treatment after 550°C PMA at N_2 ambient for 30s. The interface state density was measured using frequency-dependent conductance method. For the samples with $(NH_4)_2S$ treatment, D_{it} of 4.8×10^{11} cm^{-2}/eV at midgap is obtained, which is lower than those reported using surface nitridation [2-4]. For the samples without $(NH_4)_2S$ treatment, D_{it} is 1.4×10^{12} cm^{-2}/eV at midgap for samples with 450°C PMA. The improved interface properties in S-treated samples can be possibly explained as the GeOS interfacial layer which may suppress the Ge out-diffusion due to less Ge-O bonds and provide more stable interface properties, whereas for the samples without S passivation, the surface consists of GeO_x and it may enhance Ge out-diffusion [6] and results in poor interface property.

To understand thermal stability of S passivation, PMA at different temperature was carried out. EOT values were extracted by fitting the *C-V* data, using low frequency curves (1kHz) in accumulation which are the least affected by series or shunt resistance [7] and are summarized in Fig 4. It can be seen that samples with S passivation have thinner EOT, which indicates a larger k value of dielectric or the thinner interfacial layer than those without S passivation. The decrease of EOT values after higher temperature PMA is due to the high-k densification. Further, D_{it} values for the samples with different surface treatments and PMA temperatures are summarized in Table.1. The D_{it} degrades significantly (~2.7×10^{12} cm^{-2}/eV) for the samples without S passivation after higher temperature (550ºC) PMA, while it shows little difference for the samples with S passivation. The D_{it} values of samples without S passivation increase after higher temperature PMA is due to more Ge out-diffusion at Ge/high-k interface [8]. Thus, S passivation improves the thermal stability of Ge gate stack.

Fig 5 and 6 shows the gate leakage characteristics of Ge MOS capacitors. Both samples with S passivation or without have low gate leakage current density about 1×10^{-6}A/cm^2@V_g-V_{fb}=1V. Though samples without S passivation have larger EOT values but this does not improve the gate leakage current. This may due to the poor quality of germanium oxide interfacial layer. The cumulative probability of gate leakage density is plotted in Fig 7. It was found that the gate leakage current decreases and the distribution become more uniform, after the higher temperature (550°C) annealing, especially for the sulfur passivated samples. This is because higher temperature annealing can densify the gate dielectric and reduce the bulk traps in the gate oxide as well as weak points. The improvement in gate leakage after higher temperature annealing is less effective for samples without S passivation because of more Ge out-diffusion at elevated temperature.

4. Conclusion

The effects of the sulfur passivation of Ge using $(NH_4)_2S$ have been investigated. It was found that S passivation can effectively reduce the interface state density and improve the electrical properties in terms of EOT and gate leakage. XPS analysis shows that $(NH_4)_2S$ treatment can reduce Ge-O bonds on the Ge surface. The thermal stability of the sulfur passivation was also examined and it was found that samples with $(NH_4)_2S$ treatment exhibit stable Ge/high-k interface upon 550°C post metal deposition annealing, while interface quality degraded for those samples without sulfur passivation. This is possibly due to less Ge diffusion into high-k dielectric after sulfur passivation.

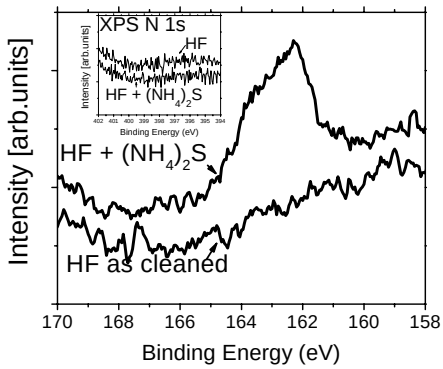

Fig 1 XPS data in S 2p after HF clean compared with HF + $(NH_4)_2S$ treatment. Inset shows there is no introduction of N on the surface after HF or $(NH_4)_2S$ treatment.

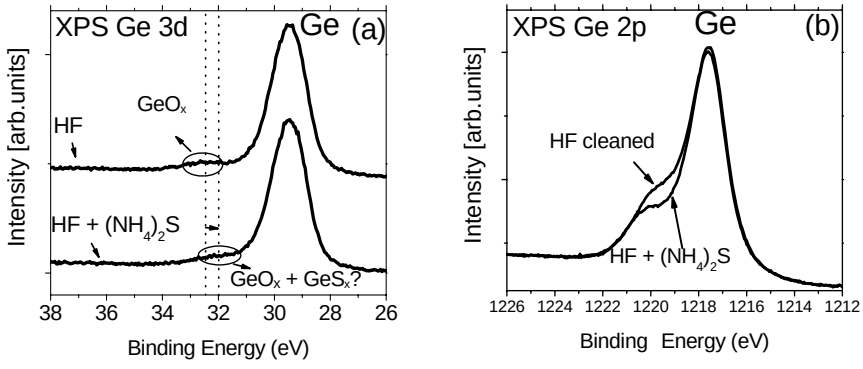

Fig 2 XPS data in **(a)** Ge 3d **(b)** Ge 2p of Ge(100) after HF clean compared with HF + $(NH_4)_2S$ treatment. The main peaks in the two graphs are corresponding Ge metallic from substrate. It can be seen that S passivation can reduce Ge-O bonds at Ge surface.

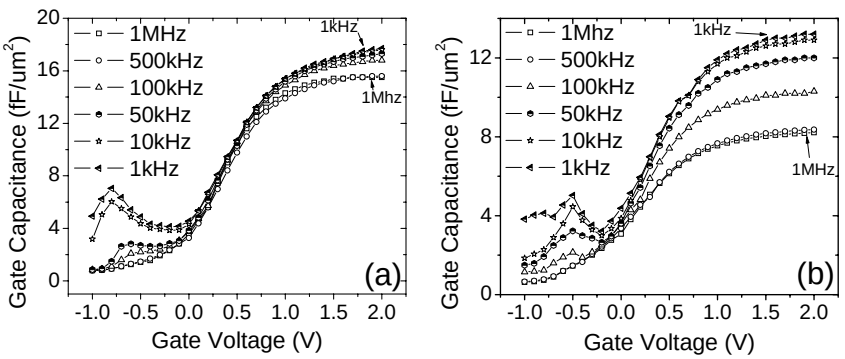

Fig 3 Capacitance-Voltage characteristics of TaN/HfON/Ge capacitors **(a)** with, **(b)**without $(NH_4)_2S$ treatment, after a 550°C PMA, in N_2 ambient for 30s. S passivated samples have much smaller frequency dispersion in accumulation region.

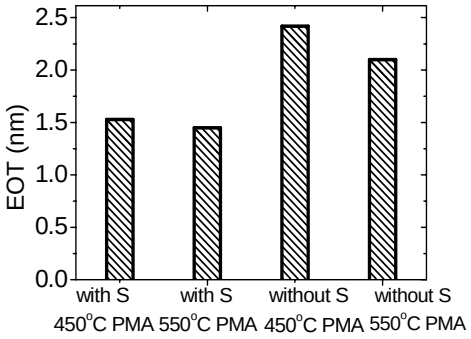

Fig 4 EOT values with different surface treatments and post metal annealing temperatures. S passivated samples show about 7Å thinner EOT.

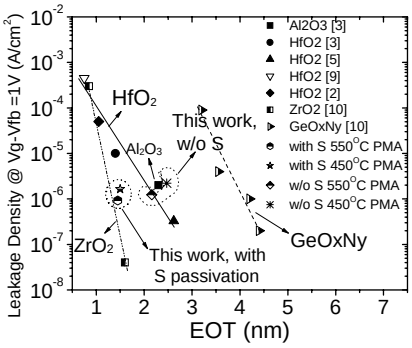

Fig 5 Gate leakage current density @Vg-Vfb =1V as a function of EOT with different surface treatments and PMA temperatures together with published data. [2-3,5,9,10].

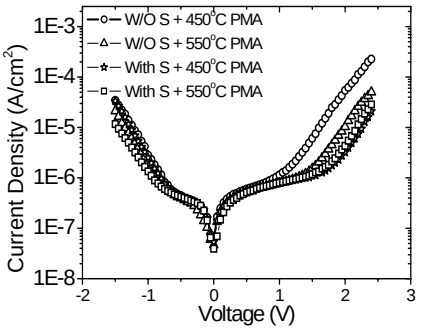

Fig 6 Typical Ig-Vg curves of Ge MOS capacitors with different surface treatments and PMA temperatures. Though S passivated samples have much smaller EOT, they exhibit comparable or even smaller gate leakage in accumulation region.

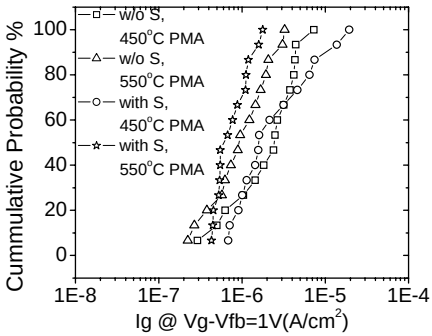

Fig 7 Cumulative probability of gate leakage current densities of Ge MOS Capacitors with different surface treatments and PMA temperatures. Most uniform distribution obtained for S passivated samples after 550ºC PMA.

Table.1 Summery of D_{it} (unit: cm^{-2}/eV) values for samples with different surface treatments and PMA temperatures at midgap. S passivated samples exhibit much smaller interface state density and better thermal stability than control samples.

	450°C PMA	550°C PMA
With S passivation	4.8×10^{11}	5.0×10^{11}
Without S passivation	1.4×10^{12}	2.7×10^{12}

References

[1] Huiling Shang, et al., *IEDM Tech. Dig.*, 2002.
[2] N. Wu, et al., *Appl. Phys. Lett.* **84** (2004) 3741.
[3] J. J. –H, et al., *IEEE Trans. Electron Devices*, **51** (2004) 1441.
[4] Martin. M. Frank et al., *Appl. Phys. Lett.* **89** (2006) 112905.
[5] C. O. Chui et al., *IEEE Electron Device Letters*, **25** (2004) 274.
[6] N. Lu et al., *Appl. Phys. Lett.* **87** (2005) 051922.K.
[7] J. Yang et al., *IEEE Trans. Electron Devices*, **85** (2004) 2902.
[8] Q. C. Zhang et al., *J. Electrochem Soc*, **153** (2006) 207.
[9] A. Dimoulas et al., *Appl.Phys. Lett.* **86** (2005) 032908.
[10] C. Chui et al., *IEEE Trans. Electron Devices*, **53** (2006) 1509.